

DTIC FILE COPY

HUGHES

2

SANTA BARBARA RESEARCH CENTER
a subsidiary

AD-A217 986

NRL HYBRID RELIABILITY

DTIC
ELECTE
FEB 14 1990
S D D

PHYSICS OF FAILURE INITIAL STUDY

FINAL REPORT FOR
PERIOD 1 OCTOBER 1986 TO 30 SEPTEMBER 1988

CONTRACT NO. N00014-86-C-2553

SANTA BARBARA RESEARCH CENTER
75 COROMAR DRIVE
GOLETA, CA 93117

DISTRIBUTION STATEMENT A
Approved for public release
Distribution Unlimited

SBRC REFERENCE No. 90-0045
DM B767-001
JANUARY 1990

90 02 13 099

SANTA BARBARA RESEARCH CENTER

A Subsidiary of Hughes Aircraft Company

75 COROMAR DRIVE, GOLETA, CALIFORNIA

NRL HYBRID RELIABILITY PHYSICS OF FAILURE INITIAL STUDY

FINAL REPORT FOR
PERIOD 1 OCTOBER 1986 TO 30 SEPTEMBER 1988

Contract No. N00014-86-C-2553

January 1990

STATEMENT "A" per W. Schmidt
NRL/Code 6813
TELECON 2/14/90

CG



Accession For	
NTIS CRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By <i>per call</i>	
Distribution /	
Availability Codes	
Dist	Availability or Special
<i>A-1</i>	

CONTENTS

<u>Section</u>	<u>Page</u>
1 INTRODUCTION.....	1-1
1.1 Objective.....	1-1
1.2 Background.....	1-1
1.3 Period of Performance	1-1
1.4 Outline of Report.....	1-1
2 INITIAL THERMAL CYCLE TESTING.....	2-1
2.1 Introduction.....	2-1
2.2 Thermal Cycle Results	2-1
2.3 Failure Analysis.....	2-4
2.3.1 Interconnect Failure Mechanism.....	2-5
2.3.2 Device Degradation Mechanism.....	2-5
2.4 Summary.....	2-8
3 INDIUM CREEP TESTING.....	3-1
3.1 Introduction.....	3-1
3.2 Testing.....	3-1
3.3 Test Results and Discussion	3-4
3.4 Conclusions.....	3-4
4 DIAGNOSTIC TECHNIQUE EVALUATION.....	4-1
4.1. Introduction.....	4-1
4.2 Dislocation Etch Study and Metal/SiO ₂ Removal.....	4-2
4.2.1 Testing Dislocation Revealing Etch.....	4-2
4.2.2 Preparing Samples for Evaluation	4-2
4.3 Results and Discussion.....	4-3
4.3.1 Reduced Electrical (I-V) Diode Response.....	4-3
4.3.2 Material Characterization Techniques	4-4
4.4 Conclusions and Recommendations.....	4-7
4.4.1 Conclusions.....	4-7
4.4.2 Recommendations.....	4-7
5 EFFECTS OF STRESS ON HFPA RELIABILITY.....	5-1
5.1 Introduction.....	5-1
5.2 Evaluation of Relationship between Dislocation Etch-pit Density and I-V Characteristics.....	5-3
5.2.1 Manually Induced Damage	5-3

CONTENTS (Continued)

<u>Section</u>		<u>Page</u>
5.2.2	Hybridization.....	5-3
5.2.3	Electrical Testing	5-4
5.2.4	Cold-weld Evaluation.....	5-4
5.2.5	SEM Etch-pit Analysis.....	5-4
5.3	Evaluation of Correlation between Hybridization Pressure and Detector Diode Damage	5-4
5.3.1	Hybridization	5-4
5.3.2	Electrical Testing	5-5
5.3.3	Indium Squeeze-out Evaluation.....	5-5
5.3.4	SEM Etch-pit Analysis.....	5-5
5.4	Evaluation of Correlation between Thermal Cycles and Detector Diode Damage.....	5-6
5.4.1	Hybridization	5-6
5.4.2	Electrical Testing	5-6
5.4.3	Cold-weld Evaluation.....	5-6
5.4.4	SEM Etch-pit Analysis.....	5-6
5.5	Etch-pit Density and Electrical Performance of Manually Damaged Arrays	5-7
5.5.1	Increased Etch-pit Density near Induced Damage	5-7
5.5.2	Degraded Electrical Performance near Induced Damage.....	5-7
5.5.3	Increased Etch-pit Density and Degraded Electrical Performance Correlation.....	5-10
5.6	Diode Stress Resulting from Hybridization at Various Pressures.....	5-10
5.6.1	Indium-bump-limited Hybridization Stress.....	5-10
5.6.2	Hybridization-induced Etch-pit Density.....	5-11
5.6.3	Effects of Hybridization on Electrical Performance	5-17
5.7	Thermal Cycling Results.....	5-19
5.7.1	Etch-pit Density.....	5-19
5.7.2	Electrical Performances.....	5-19
5.8	Conclusions.....	5-22
6	SUMMARY AND CONCLUSIONS	6-1
6.1	Initial Thermal Cycle Study.....	6-1
6.2	Indium Creep Testing	6-1
6.3	Diagnostic Technique Evaluation	6-1
6.4	Effects of Stress on HFPA Reliability	6-2

CONTENTS (Continued)

Appendix

A	DISLOCATION ETCH MICROGRAPHS.....	A-1
B	I-V CURVES AFTER 25 AND 200 THERMAL CYCLES.....	B-1
C	DIODE MAPPING LOCATIONS BY ASSEMBLY	C-1
D	SEM MICROGRAPHS OF INDIVIDUAL DIODES TO FANOUTS.....	D-1
E	PALLADIUM ETCH RESULTS.....	E-1
F	AFTER PALLADIUM AND DISLOCATION ETCHES	F-1
G	X-RAY ANALYSIS DATA.....	G-1

ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
2-1	60 × 3 (12) LWIR HgCdTe Array Is Structurally Similar in Length of Its Maximum Dimension (Diagonal) to 128 × 128 Array.....	2-1
2-2	Percent Operability for Indium Bump Interconnects and Detector IR Response versus Cumulative Thermal Cycles (Assembly 5089).....	2-2
2-3	Gray-scale Map Showing Operability of Indium Bump Interconnects (Warm and Cold) and Detector IR Response after 7 Cumulative Thermal Cycles (Assembly 5089)	2-3
2-4	Gray-scale Map Showing Operability of Indium Bump Interconnects (Warm and Cold) and Detector IR Response after 40 Cumulative Thermal Cycles (Assembly 5089)	2-3
2-5	Gray-scale Map Showing Operability of Indium Bump Interconnects (Warm and Cold) and Detector IR Response after 81 Cumulative Thermal Cycles (Assembly 5089)	2-4
2-6	Schematic of Cross Section of Individual Pixel on Hybrid Array Showing Possible Failure Mechanisms Induced by Thermal Cycling.....	2-5
2-7	(a) Gray-scale Map Showing Operability of Indium Bump Interconnects after 81 Cumulative Thermal Cycles (Assembly 5089). (b) SEM Micrograph of Pixels (after pulling apart hybrid) of Good Interconnects in Interior of Array Showing Good Indium Bump Cold-welding Characteristics. (c) SEM Micrograph Showing Interconnect Delamination at Contact Metal/HgCdTe Interface. (d) SEM Micrograph of Many Pixels Showing Interconnect Delamination	2-6
2-8	(a) Gray-scale Map Showing Detector IR Response Uniformity after 81 Cumulative Thermal Cycles (Assembly 5089). (b) SEM Micrograph of Pixels (after pulling apart hybrid) Showing Poor IR Response Due to Passivation Layer Delamination.....	2-7
3-1	Overall Specimen-holding Fixture.....	3-2
3-2	Close-up of Test Specimen in Holding Fixture.....	3-3
3-3	Room-temperature Creep Tests at 294K	3-5
3-4	Dry-ice and Acetone Creep Tests at 189K.....	3-6
3-5	Liquid-nitrogen Creep Tests at 77K	3-7
4-1	Architecture Layers of Diode	4-3
4-2	Cracks Appeared in Assembly 6509 Even before Dislocation Etch.....	5-6
5-1	Increased Etch-pit Density near Induced Damage	5-8
5-2	Degraded Electrical Performance near Manually Induced Damage	5-9
5-3	Hybridization Stress Buffered by Cold Flow Characteristics at Indium Bumps.....	5-12
5-4	Etch-pit Density Not Increased by Hybridization Forces between 0 and 120 lb	5-13

ILLUSTRATIONS (Continued)

<u>Figure</u>		<u>Page</u>
5-5	Indium Squeeze-out Due to Hybridization Force Gradient.....	5-15
5-6	Increased Etch-pit Density Due to a Hybridization Force in Excess of 120 lb.....	5-16
5-7	Open-field-of-view Electrical Performance Unchanged by Hybridization at 35 lb.....	5-18
5-8	Zero Field-of-view Electrical Performance Unchanged by Hybridization at 35 lb.....	5-20
5-9	Etch-pit Density Not Affected by 200 Thermal Cycles.....	5-21

TABLES

<u>Table</u>		<u>Page</u>
3-1	Data for 294K Creep Tests.....	3-8
3-2	Data for 189K Creep Tests.....	3-8
3-3	Data for 77K Creep Tests.....	3-8
4-1	Number of Thermal Cycles Experienced by Each Assembly.....	4-1
4-2	Testing Parameters Used for I-Vs.....	4-3
4-3	Thermal Cycle and I-V History for Each Assembly.....	4-4
4-4	Hybrid and Pull (Tensile) Force for Each Assembly.....	4-5
5-1	Correlation between Increased Etch-pit Density and Degraded I-V Characteristics Due to Intentionally Induced Damaged	5-11
5-2	IRFPA Stress Not strongly Affected by Increased Hybridization Force	5-14
5-3	Etch-pit Density Versus Hybridization Force	5-17
5-4	Thermal Cycle Results.....	5-19

Section 1 INTRODUCTION

1.1 OBJECTIVE

The objective of this program was to identify the failure mechanisms associated with the thermal cycling of HgCdTe hybrid infrared focal plane arrays from room temperatures to cryogenic temperature (typically 77K). This work included evaluating the possible occurrence of damage (increased dislocation density, fracturing, etc.) in the HgCdTe as a result of the hybridization process and/or thermal cycling.

1.2 BACKGROUND

Infrared focal-plane arrays (IRFPAs) produced at SBRC are hybrid structures consisting of a HgCdTe infrared-sensitive material subdivided into an array of photodiodes and connected, via a matrix of indium interconnects or "bumps," to a silicon readout used to collect the charge generated in the HgCdTe as a result of the IR signal. The readout output can be used to generate an IR image.

There is a concern in the IR community that the long-term reliability of IRFPAs may be in question due to defects being formed as a result of the hybridization process and/or thermal cycling of the arrays from room to cryogenic temperatures. This report summarizes the initial work directed at answering these questions.

1.3 PERIOD OF PERFORMANCE

The funding for this program was incremental and limited and contract work was performed within the following periods;

1. October 1986 – July 1987
2. May 1988
3. August 1988

1.4 OUTLINE OF REPORT

Section 2 summarizes the initial results on identifying the failure modes associated with thermal cycling PV HgCdTe hybrid detector arrays. Section 3 details a small effort on indium creep testing. Section 4 covers work done to define and develop diagnostic techniques to monitor changes in HgCdTe induced by stress. Section 5 summarizes the efforts to quantify the effect of damage induced into HgCdTe as a result of the hybridization process and thermal cycling and its effect on the detector I-V characteristics. Finally, Section 6 gives the summary and conclusions of this work and recommendations for further work.

Section 2

INITIAL THERMAL CYCLE TESTING

2.1 INTRODUCTION

The objective of this task was to obtain some initial data on the failure modes associated with PV HgCdTe hybrid arrays. As a vehicle for this testing a 160×3 (12) LWIR HgCdTe array hybridized to a Si readout was used. This hybrid is structurally similar in the length of its maximum dimension (diagonal) to a 128×128 array, as shown in Figure 2-1.

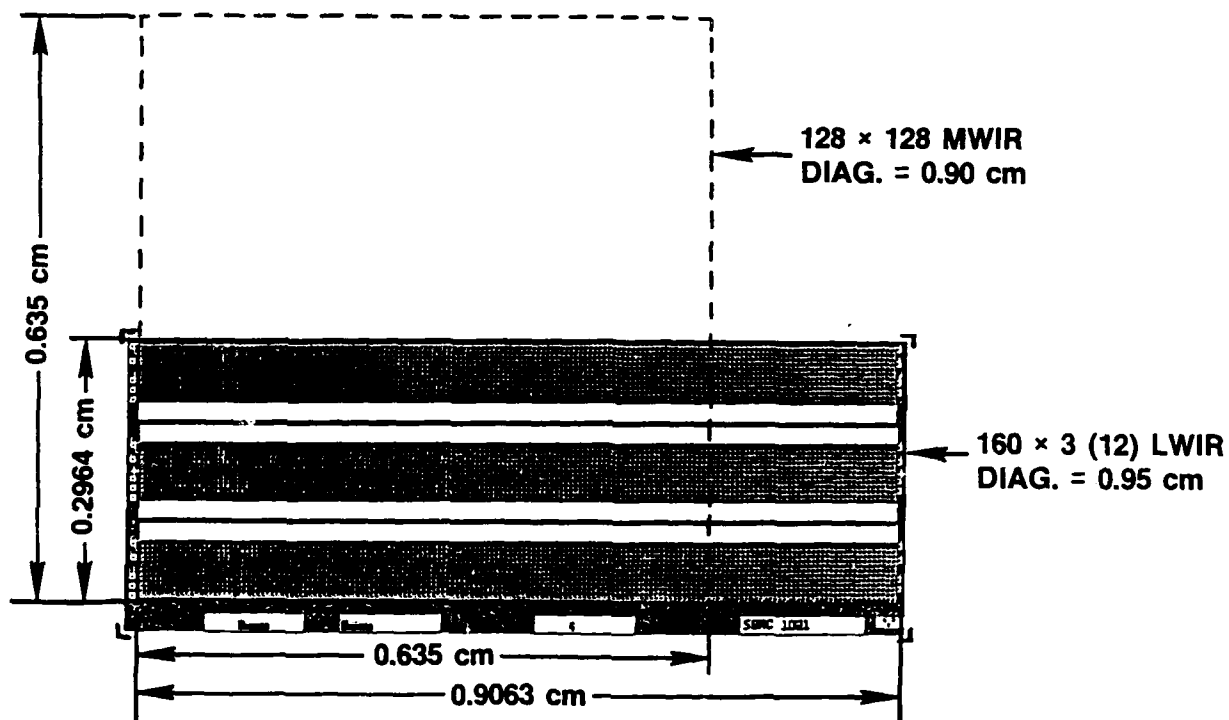


Figure 2-1. 160×3 (12) LWIR HgCdTe Array Is Structurally Similar in Length of Its Maximum Dimension (Diagonal) to 128×128 Array

2.2 THERMAL CYCLE RESULTS

The 160×3 (12) LWIR HgCdTe hybrid array (assembly 5089) was first tested then thermally cycled from room temperature to liquid nitrogen temperature (300K to 77K) in an environmental chamber. The array was tested at 77K after 7, 20, 40, and 81 cumulative temperature cycles. To separate effects associated with indium bump delamination from those effects due to detector degradation, the continuity of the indium bump interconnects was measured at 300K to

determine which diodes had opened up prior to detector testing, thus showing no IR response when tested at 77K.

Figure 2-2 shows a plot of percent operability versus number of cumulative thermal cycles. One curve shows indium bump interconnect operability and the other curve shows detector response operability. Figure 2-2 shows that the interconnects began to fail at approximately 40 cumulative thermal cycles. Detector operability was initially 73% and degraded to 60% after 7 cycles; further degradation with thermal cycling was associated with interconnect reliability.

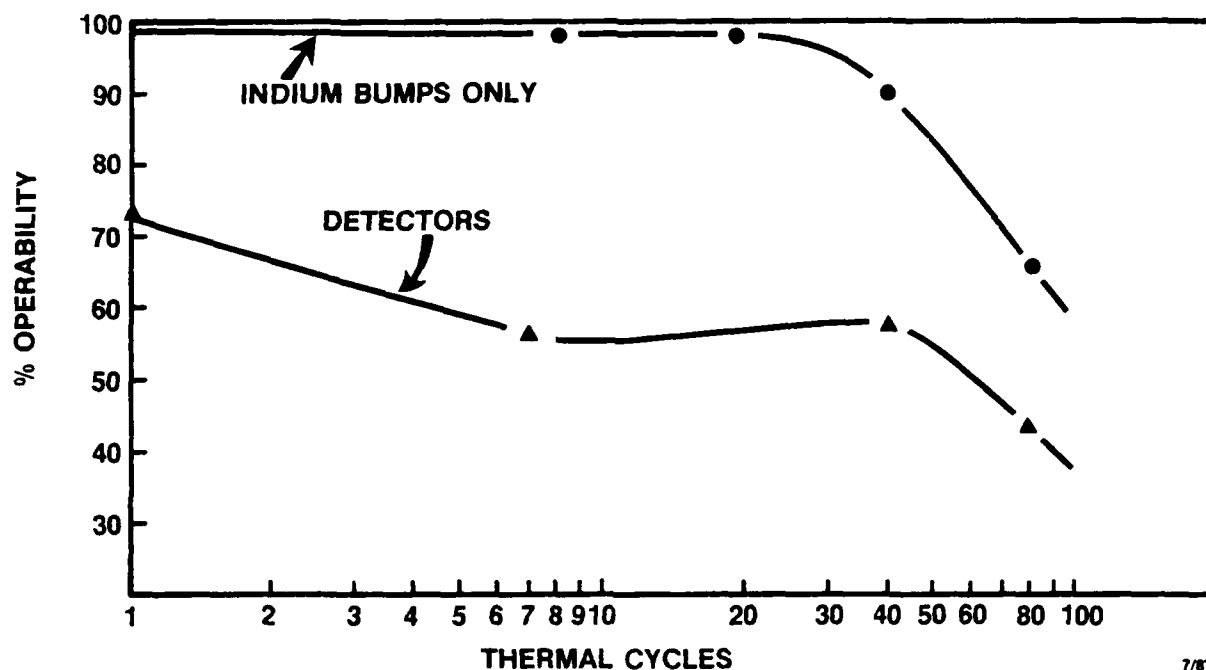

 7/87
 71432-25

Figure 2-2. Percent Operability for Indium Bump Interconnects and Detector IR Response versus Cumulative Thermal Cycles (Assembly 5089)

A more detailed look at these results is shown in Figures 2-3, 2-4, and 2-5, which show a gray scale map of indium interconnect operability at 300K and 77K and detector IR response at 77K, after 7, 40, and 81 cumulative cycles, respectively. Figure 2-3 shows that the interconnect reliability is good, but that the IR detector response operability is degraded. Figures 2-4 and 2-5 show that the indium bump interconnects are degrading with thermal cycling and the detector response is degraded only as a result of this interconnect loss. Scanning electron microscopy was used to analyze these degradation mechanisms and is discussed in the next section.

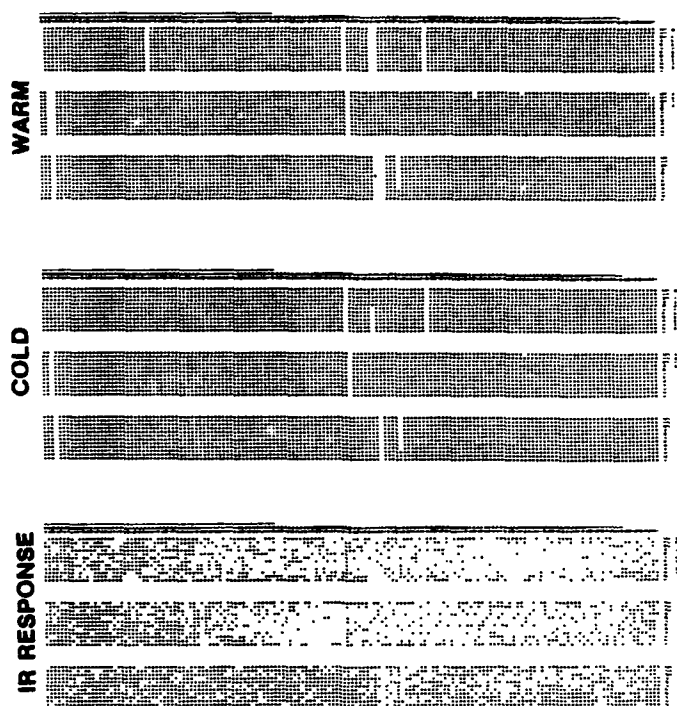


Figure 2-3. Gray-scale Map Showing Operability of Indium Bump Interconnects (Warm and Cold) and Detector IR Response after 7 Cumulative Thermal Cycles (Assembly 5089)

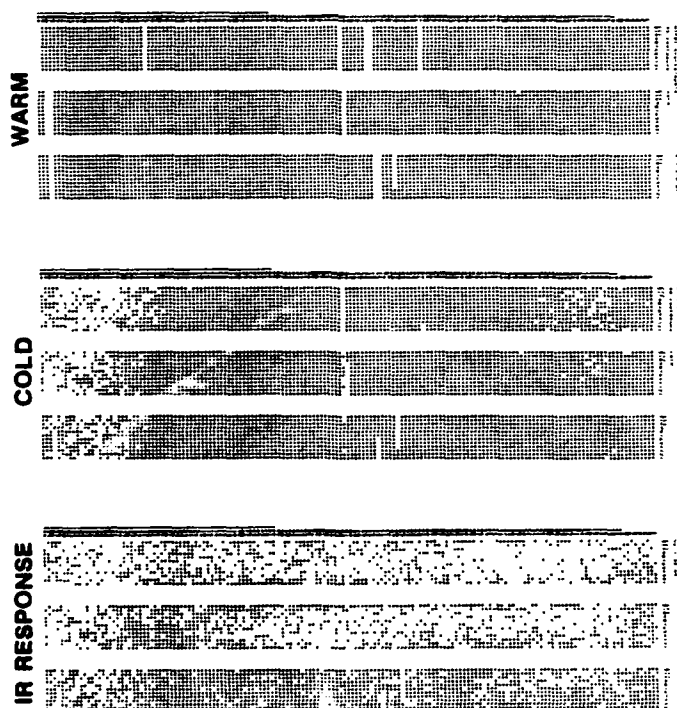


Figure 2-4. Gray-scale Map Showing Operability of Indium Bump Interconnects (Warm and Cold) and Detector IR Response after 40 Cumulative Thermal Cycles (Assembly 5089)

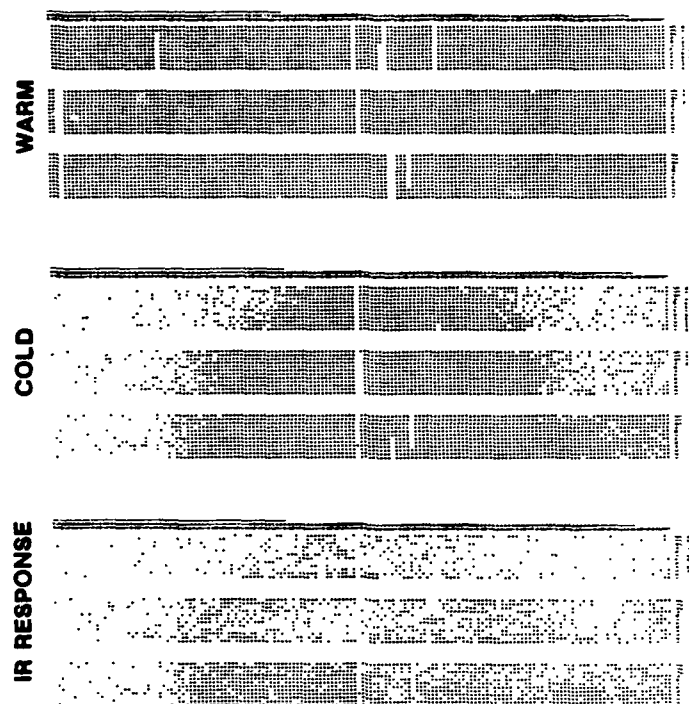


Figure 2-5. Gray-scale Map Showing Operability of Indium Bump Interconnects (Warm and Cold) and Detector IR Response after 81 Cumulative Thermal Cycles (Assembly 5089)

2.3 FAILURE ANALYSIS

Figure 2-6 is a schematic of a cross-section of an individual pixel in a hybrid array and shows possible failure mechanisms induced by thermal cycling. The following failure mechanisms can occur:

Interconnect Failures

1. In/In interface
2. In/HgCdTe contact interface
3. Contact/HgCdTe interface
4. In/Si contact interface

Device Degradation

1. HgCdTe material degradation
2. Passivation degradation

The hybrid assembly was pulled apart and analyzed in the SEM to determine which of these failure mechanisms was present.

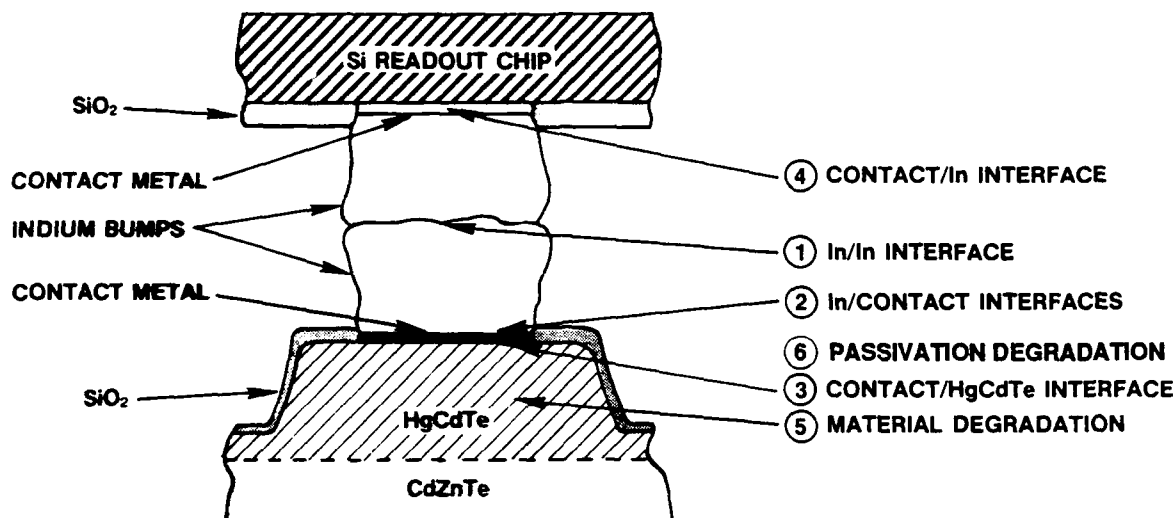


Figure 2-6. Schematic of Cross Section of Individual Pixel on Hybrid Array Showing Possible Failure Mechanisms Induced by Thermal Cycling

2.3.1 Interconnect Failure Mechanism

Figure 2-7a shows the gray scale map of interconnect failure of the 160×3 (12) LWIR HgCdTe hybrid array (Assembly 5089) after 81 cumulative thermal cycles; Figures 2-7b, c, and d are SEM micrographs of the array after it was pulled apart for analysis. Figure 2-7b shows an SEM micrograph of several pixels in the central region of the hybrid which showed good interconnect operability. The indium bumps showed good cold welding characteristics in this region, as evidenced by their elongated shape after pulling the array apart. Figures 2-7b and c show micrographs of pixels in the exterior region of the array which exhibited poor interconnect operability upon thermal cycling. These figures show that the dominant failure mechanism was contact delamination at the contact metal/HgCdTe interface. This was probably due to surface contamination sometime prior to the metallization step and is not an inherent process limitation.

2.3.2 Device Degradation Mechanism

Figure 2-8a shows the gray scale map of device operability of the 160×3 (12) LWIR HgCdTe hybrid array (Assembly 5089) after 81 cumulative thermal cycles and Figure 2-8b shows an SEM micrograph of several pixels on the array which showed poor IR response. Figure 2-8b shows that the SiO_2 passivation layer is lifting from the surface and is thus ineffective in passivating the array surface and results in poor uniformity of operability across the array. This again was probably due to surface contamination prior to the passivation step and is not an inherent process limitation.

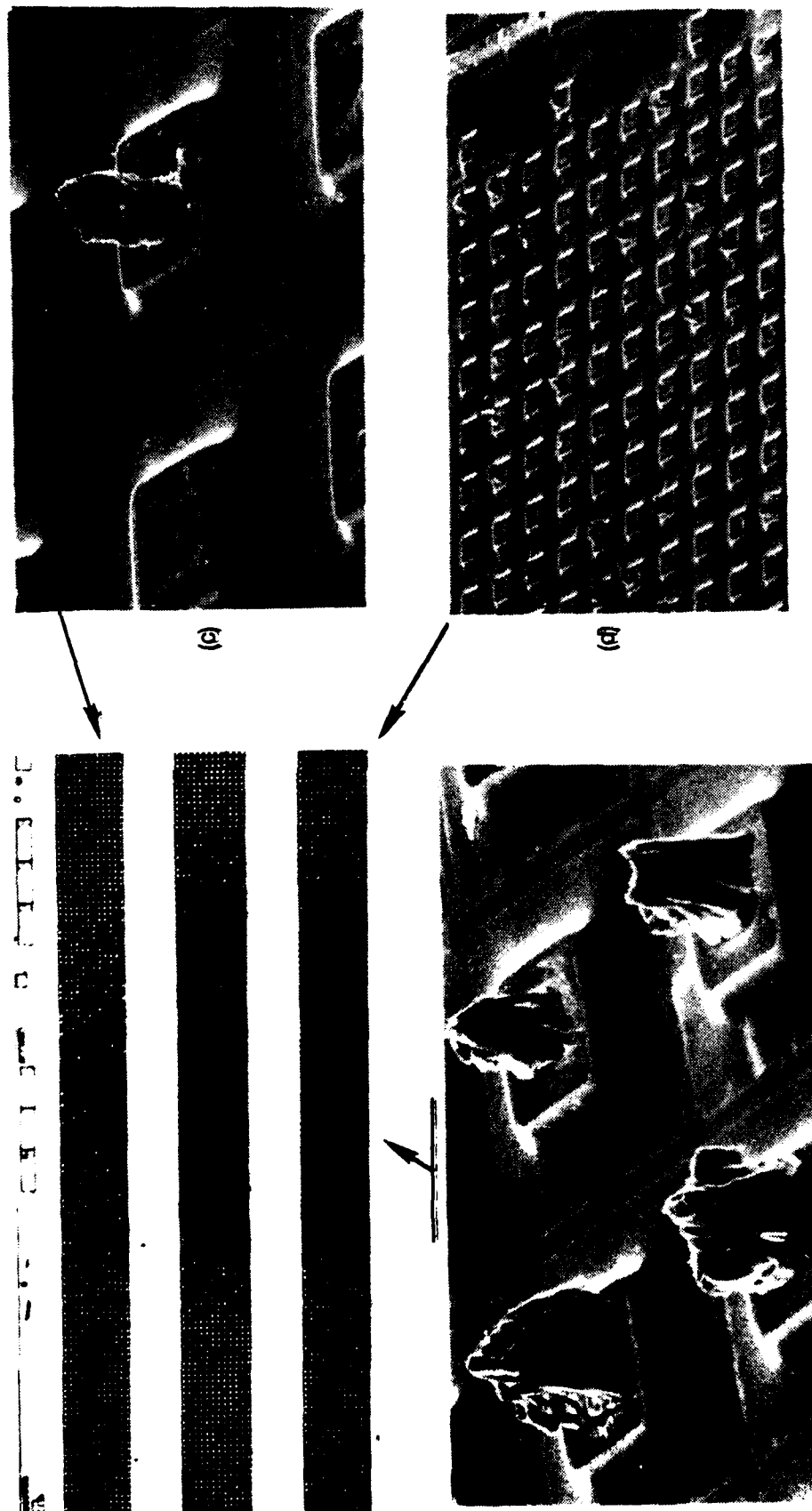


Figure 2-7. (a) Gray-scale Map Showing Operability of Indium Bump Interconnects after 81 Cumulative Thermal Cycles (Assembly 5089). (b) SEM Micrograph of Pixels (after pulling apart hybrid) of Good Interconnects in Interior of Array Showing Good Indium Bump Cold-welding Characteristics. (c) SEM Micrograph Showing Interconnect Delamination at Contact Metal/HgCdTe Interface. (d) SEM Micrograph of Many Pixels Showing Interconnect Delamination.

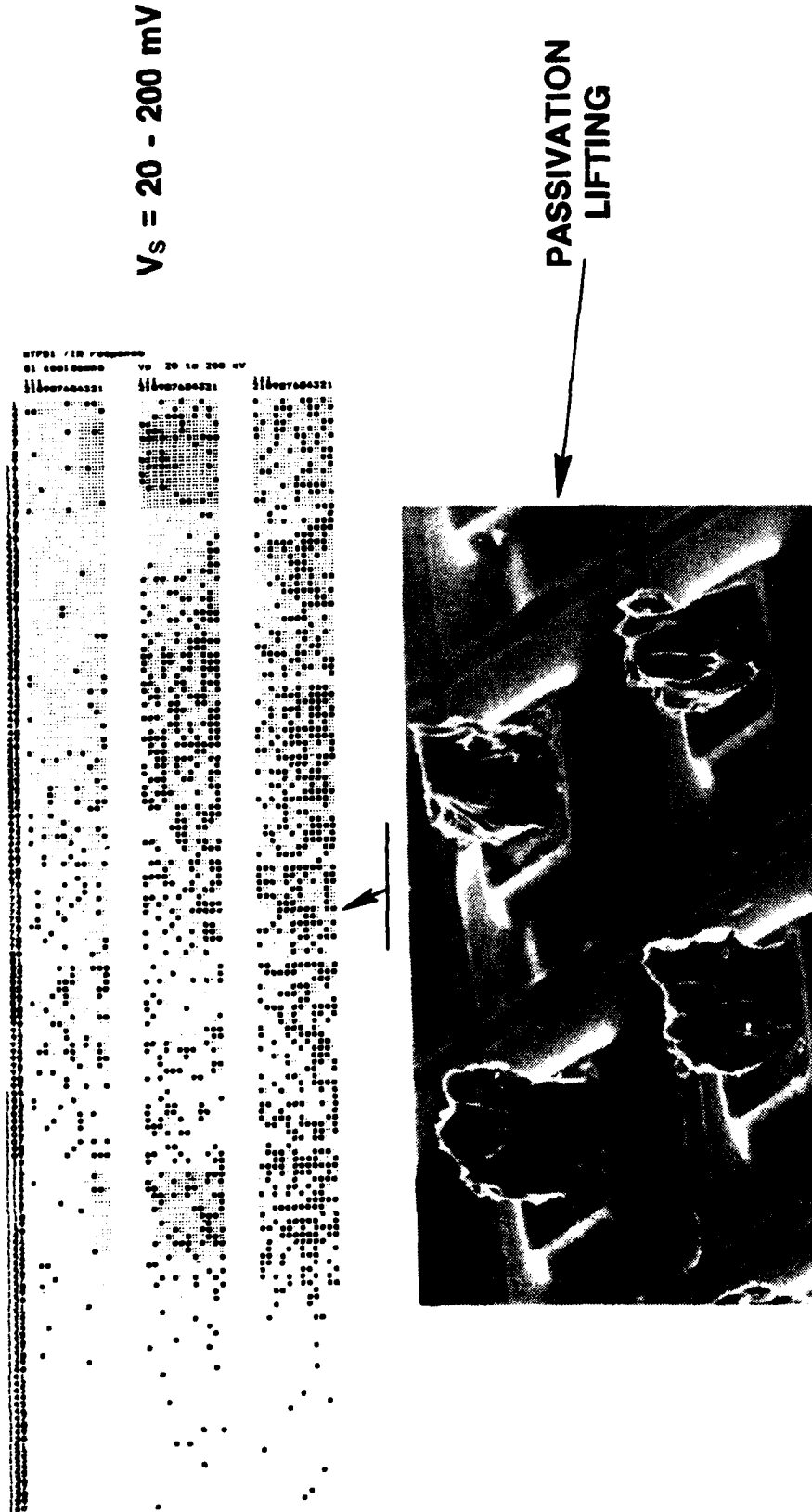


Figure 2-8. (a) Gray-scale Map Showing Detector IR Response Uniformity after 81 Cumulative Thermal Cycles (Assembly 5089). (b) SEM Micrograph of Pixels (after pulling apart hybrid) Showing Poor IR Response Due to Passivation Layer Delamination.

2.4 SUMMARY

An initial study was made to identify the failure modes associated with thermal cycling PV HgCdTe hybrid arrays. As a vehicle for this testing, a 160×3 (12) LWIR HgCdTe array hybridized to a Si readout was tested and thermal cycled up to a cumulative total of 81 thermal cycles. The hybrid was then pulled apart and analyzed in the SEM. Two primary failure modes were identified:

1. Interconnect failure due to delamination at the contact metal/HgCdTe interface
2. Passivation delamination from HgCdTe surface causing device degradation

These failures were apparently due to unwanted surface contamination during the processing of this device and are not inherent limitations to hybrid detector arrays. These problems have been eliminated in the process and did not affect further experiments discussed in the next sections.

Section 3

INDIUM CREEP TESTING

3.1 INTRODUCTION

Three lap shear specimens with pure indium as the bond material were tested to determine the creep properties of indium in shear, at three temperatures and three stress levels. The reason for this testing was to obtain data for failure modeling of indium interconnect bumps between a detector array and a readout. The thickness of the interconnecting bumps is 15 to 20 μm . The test apparatus and specimen configuration which were used to test the creep properties of the indium in shear are shown in Figures 3-1 and 3-2. For the low temperature tests, the specimens were immersed in a dewar containing liquid nitrogen or dry ice and acetone.

3.2 TESTING

Creep tests were performed in room temperature air (294K), in dry ice and acetone (189K), and in liquid nitrogen (77K). The temperature of the dry ice and acetone was monitored with a copper-constantan thermocouple during the tests. Indium bond thicknesses for the three specimens were 47.8 μm for the room temperature specimen, 56.6 μm for the dry ice and acetone specimen, and 65.8 μm for the liquid nitrogen specimen. Specimens were tested at three constant loads at 294K, three constant loads at 189K, and one load at 77K. Specimens were annealed at 200°F for 30 minutes, after each creep test, in order to release any strain energy stored from prior testing. Specimen loads were measured using a standard 500 pound Instron load cell. Deformation in the indium was measured with strain gages. One gage, Figure 3-2, was placed across two pieces of rigid aluminum bonded together with indium, and measured the actual deformation in the indium during testing. The strains and strain rates reported herein equal the overall strain recorded by the gage minus the elastic deformation which occurred in the aluminum portion under the strain gage. In addition the following test conditions were imposed:

1. For testing the 189K and 77K specimens, the bond area was reduced to increase the stress in the indium for a given load, and thus accelerate the creep rate.
2. Another gage was placed on a nonloaded piece of aluminum near the test specimen and was used for temperature compensation.
3. Specimens were pulled on an Instron in tension at constant rates ranging from 0.86 $\mu\text{m}/\text{min}$ to 2.1 $\mu\text{m}/\text{min}$, and were then held at certain constant loads for periods of 20 minutes to observe the creep characteristics of indium as a function of temperature and stress.

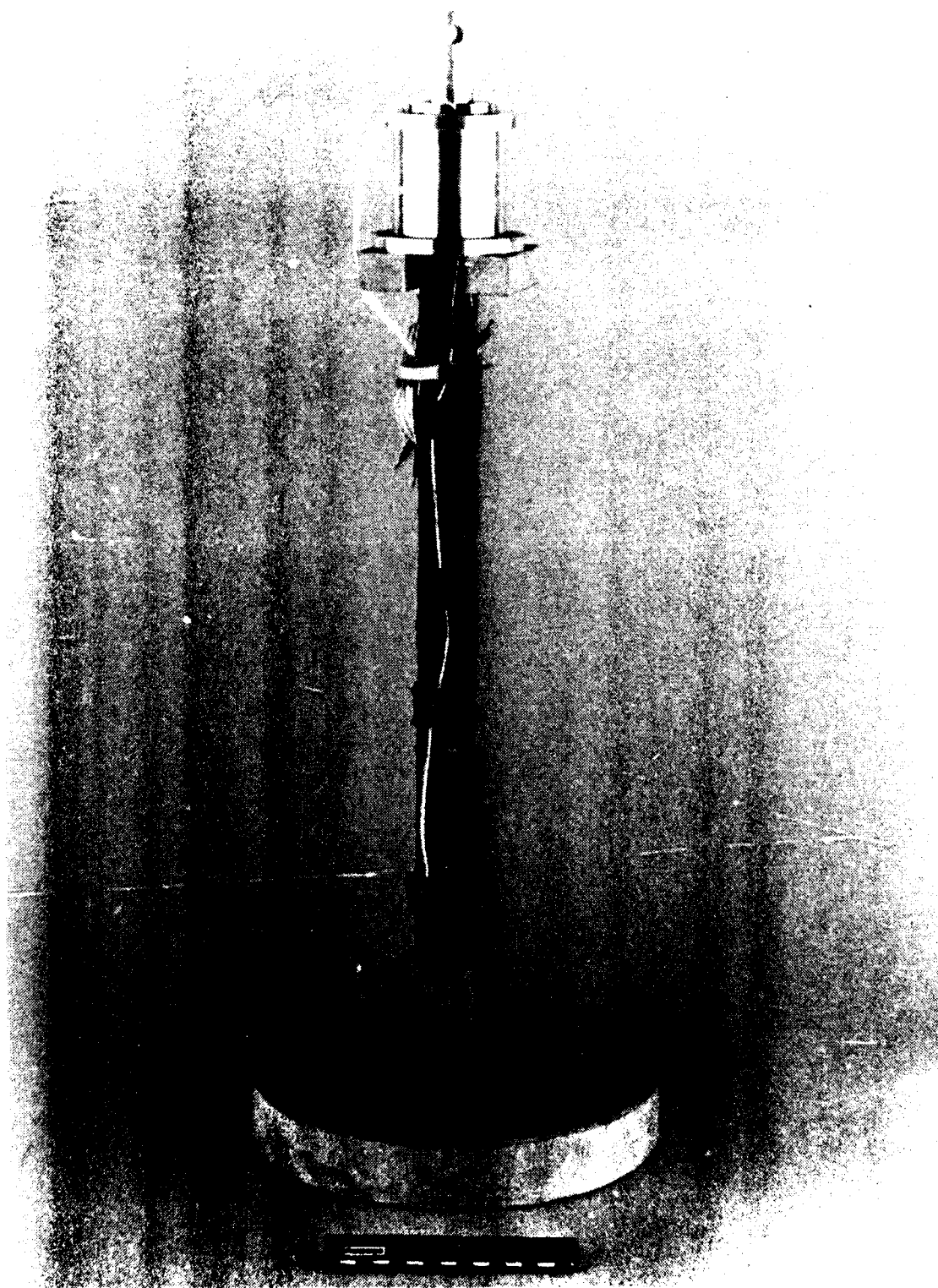


Figure 3-1. Overall Specimen-holding Fixture

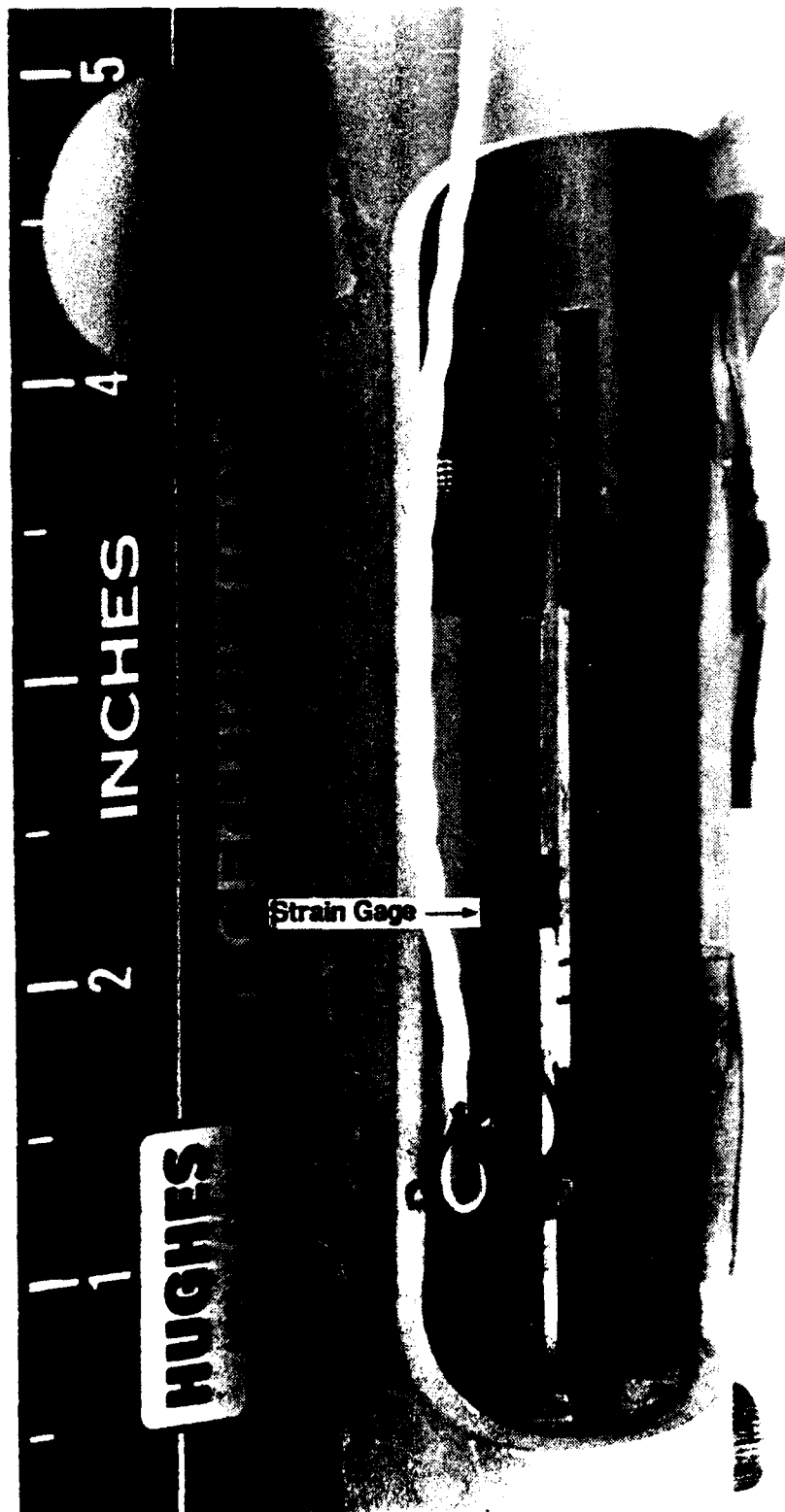


Figure 3-2. Close-up of Test Specimen in Holding Fixture

3.3 TEST RESULTS AND DISCUSSION

1. Room Temperature (294K) Test:

The creep characteristics of the specimen tested at room temperature are shown in Figure 3-3, and actual values are recorded in Table 3-1. The specimen held at 55 psi was first deformed $4.2\text{ }\mu\text{m}$ at a constant rate of $1.4\text{ }\mu\text{m/min}$, before being held at a constant stress of 55 psi for 20 minutes. The specimen held at 79 psi was first deformed to $5.6\text{ }\mu\text{m}$ at a rate of $1.4\text{ }\mu\text{m/min}$, and the specimen held at 148 psi was first deformed $8.9\text{ }\mu\text{m}$ at a constant rate of $2.1\text{ }\mu\text{m/min}$. As expected, the overall creep rate increased with increasing constant stress at room temperature.

2. Dry Ice and Acetone (189K) Tests:

The creep characteristics of the specimen tested in dry ice and acetone are shown in Figure 3-4, and actual values are recorded in Table 3-2. The specimen held at 164 psi was first deformed a total of $3.1\text{ }\mu\text{m}$ at a constant rate of $0.6\text{ }\mu\text{m/min}$. The specimen held at 205 psi was first deformed $5.0\text{ }\mu\text{m}$ at a rate of $0.9\text{ }\mu\text{m/min}$. These specimens were held at constant load for 8 minutes when the test had to be terminated due to strain gage failure. The specimen held at 687 psi was deformed $7.5\text{ }\mu\text{m}$ at a constant rate of $1.2\text{ }\mu\text{m/min}$ and held at constant stress for 20 minutes. The curve beyond 20 minutes represents the deformation that occurred as the stress was cycled from 671 psi to 703 psi for 4 cycles. Creep rate is seen to increase with increasing constant stress for the three tests. The portion of the 687 psi test from 20 to 28 minutes indicates that large deformations resulted from ± 16 psi changes in the constant stress level, and do not represent normal creep behavior.

3. Liquid Nitrogen (77K) Test:

The creep response of the specimen tested in liquid nitrogen is shown in Figure 3-5, and actual values are recorded in Table 3-3. The specimen held at 1062 psi was first deformed a total of $3.7\text{ }\mu\text{m}$ at a constant rate of $1.3\text{ }\mu\text{m/min}$, and then held for 20 minutes. The creep deformation at this stress and temperature was very low and the intermediate two minutes interval data points could not be resolved in all cases, and the overall creep for 20 minutes is plotted. This specimen was subsequently cycled from 1031 psi to 1095 psi, and the same rapid deformation with small changes in constant stress was observed similar to that in the 687 psi test at 189K.

3.4 CONCLUSIONS

1. Creep rate in the indium increases with increasing test temperature and holding stress.
2. The near linear slope of the major portion of the curves is similar to the start of second stage or steady state creep. The rapid deformation exhibited by adding a small cyclic loads to the steady state load after the 189K and 77K creep tests is not typical creep behavior.
3. Small cyclic loading and relaxation unloading around the constant holding stress also accelerates the creep rate in specimens tested at 189K and 77K.

The data determined in this study are in agreement with the data published by the National Bureau of Standards on indium. The data can be used for modeling of metallurgical processes in indium.

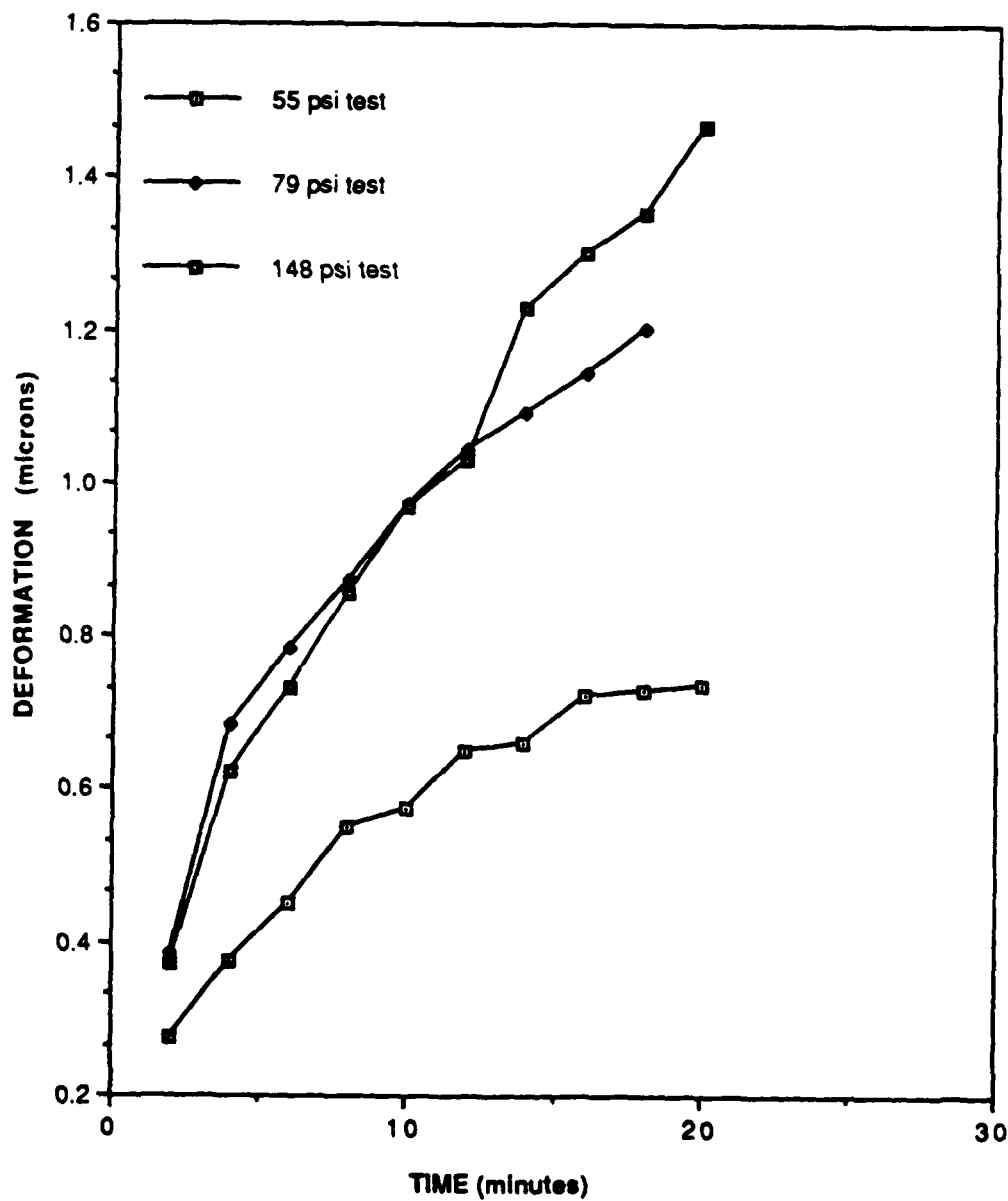


Figure 3-3. Room-temperature Creep Tests at 294K

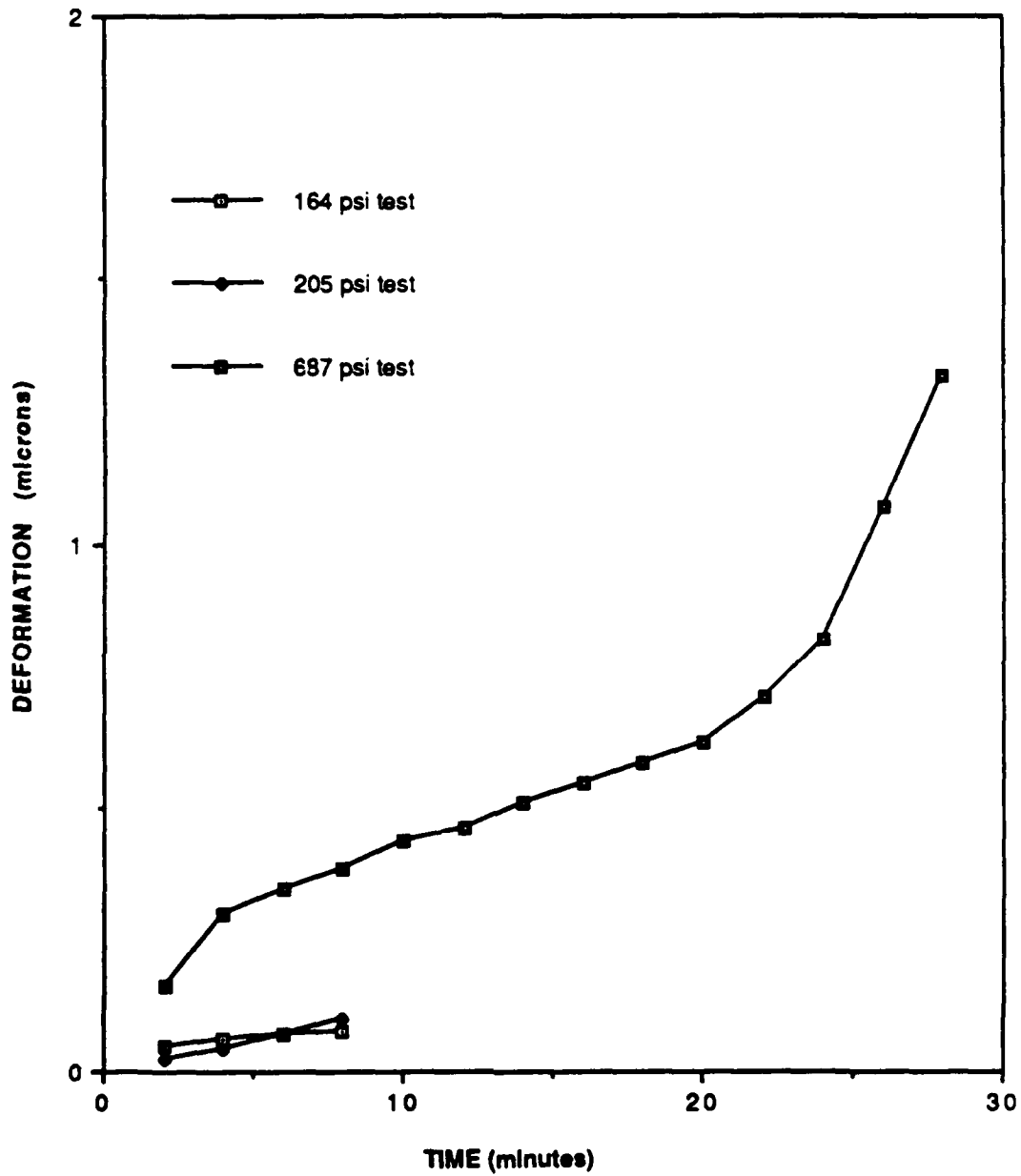


Figure 3-4. Dry -ice and Acetone Creep Tests at 189K

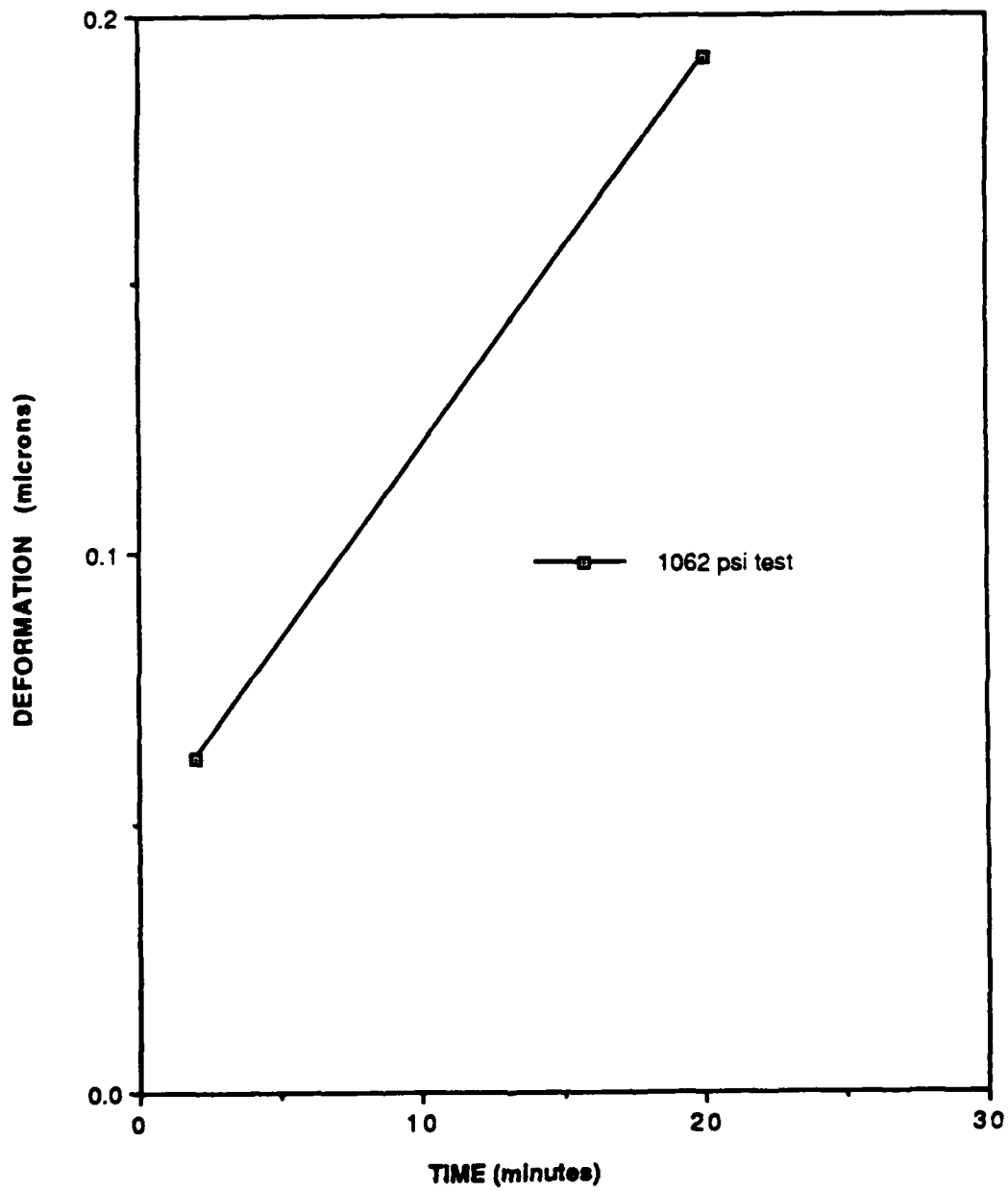


Figure 3-5. Liquid-nitrogen Creep Tests at 77K

Table 3-1. Data for 294K Creep Tests

Time (minutes)	55 psi test: Deformation (μm)	79 psi test: Deformation (μm)	147 psi test: Deformation (μm)
2	0.274	0.387	0.372
4	0.374	0.685	0.621
6	0.449	0.785	0.732
8	0.549	0.874	0.857
10	0.574	0.973	0.968
12	0.648	1.043	1.030
14	0.661	1.092	1.229
16	0.723	1.142	1.303
18	0.729	1.202	1.353
20	0.736		1.465

Table 3-2. Data for 189K Creep Tests

Time (minutes)	164 psi test: Deformation (μm)	205 psi test: Deformation (μm)	687 psi test: Deformation (μm)
2	0.047	0.025	0.161
4	0.060	0.045	0.298
6	0.070	0.070	0.348
8	0.075	0.100	0.385
10			0.435
12			0.459
14			0.509
16			0.546
18			0.584
20			0.621
22			0.708
24			0.819
26			1.068
28			1.316

Table 3-3. Data for 77K Creep Tests

Time (minutes)	1062 psi test Deformation (μm)
2	0.062
20	0.192

Section 4

DIAGNOSTIC TECHNIQUE EVALUATION

4.1. INTRODUCTION

Our goal was to define and develop appropriate diagnostic techniques to monitor changes in HgCdTe induced by stress, determine when, where, and why damage occurs, and alter processes and architectures to eliminate or minimize material degradation. To accomplish this goal we performed the following:

1. Induce reduced electrical response in diodes
2. Determine methodology to study possible material degradation associated with changes in electrical performance

Hybrids used for this study were 128 x 128 (0.25 in²) large-area staring HgCdTe detectors hybridized to sapphire fanouts capable of monitoring 60 of the 16,000 + diodes. For this study, five MWIR (mid wave infrared) n-on-p 128² hybrids were used.

Thermal cycle induced degradation was of primary interest in this study. We have shown that diode performance of large-area hybrids degrades with increasing thermal cycling, possibly due to thermally induced fatigue. Two parts were thermal cycled 200 times in an attempt to induce sufficient, measurable diode degradation.

The five parts were thermal cycled from 3 to 200 times, as shown in Table 4-1. (Each thermal cycle varies the temperature from room temperature {300K} to 95K and back up to room temperature.) To prepare for thermal cycling, the hybrids were placed in a nitrogen box, purged, and sealed in a container. They were then thermal-cycled in an environmental chamber. A minicomputer controlled the cool-down and heating of the chamber, with each complete cycle taking about one hour.

Table 4-1. Number of Thermal Cycles Experienced by Each Assembly

Assembly	Thermal Cycles
6537	3
6508	25
6131	25
6146	200
6509	200

I-V testing was done at 120K at the beginning and end of the thermal cycling. Diodes whose performance degraded were noted and analyzed.

Failure analysis was conducted on all five hybrids following thermal cycling. The study focused on individual diodes with performance changes (either better or worse) as the result of thermal cycling. Failure analysis began with tensile testing (pull test force) of the hybrid, followed by visual inspection and SEM analysis of the array, looking for any obvious degradation or failure mechanisms. Next, the indium bumps and contact metals were removed. A dislocation-revealing etch was applied, and optical and SEM analysis were conducted to monitor changes in dislocation densities. Finally, an X-ray double-crystal rocking curve analysis was performed on the substrates.

4.2 DISLOCATION ETCH STUDY AND METAL/SiO₂ REMOVAL

4.2.1 Testing Dislocation Revealing Etch

The dislocations were revealed by a combination of hydrogen peroxide and ammonium hydroxide. The "recipe" used for the dislocation revealing etch follows: (1) Soak substrates in 2:1 H₂O₂:NH₄OH for 5 to 15 minutes at room temperature. (2) Quench in de-ionized water for a few minutes and blow dry with nitrogen gas.

The first objective of the dislocation study was to show that the 2:1 solution of hydrogen peroxide and ammonium hydroxide would indeed reveal dislocations. To meet this objective, damage was intentionally induced in epitaxial HgCdTe substrates, and then these substrates were placed in the etch solution for 5, 10, 15, and 20 minutes. This etch was successful, and a second trial was conducted at 4, 6, 8, and 10 minutes to optimize the etchant. The results are documented in Appendix A. From these studies, 10 minutes was chosen to be the most appropriate etch time to use.

4.2.2 Preparing Samples for Evaluation

The next step was to strip 128² devices of their layers (metal and SiO₂) so that defect etching could be performed. The architecture of devices, with a description of the thin film layers, is shown in Figure 4-1. Stripping occurred in three steps:

1. Removal of In/Ni in HCl at room temperature for 6 minutes; intermittent agitation
2. Removal of palladium with one of two solutions:
 - a. Transene "palladium etchant" at room temperature for 10 seconds; constant agitation
 - b. Allied "PAE 16:1:1:2 etchant" at 47°C for 1 minute; constant agitation. The 16:1:1:2 etchant is composed of phosphoric acid:nitric acid:acetic acid:H₂O.

3. Removal of SiO_2 passivation with "BOE 500" HF etchant at room temperature for 45 seconds, constant agitation.

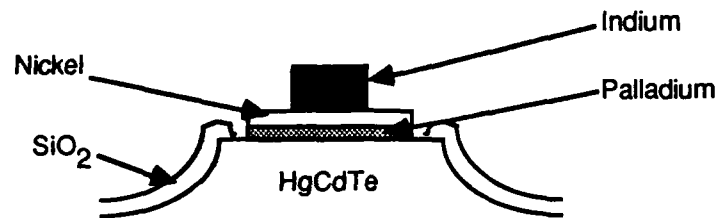


Figure 4-1. Architecture Layers of Diode

4.3 RESULTS AND DISCUSSION

4.3.1 Reduced Electrical (I-V) Diode Response

I-V characteristics were collected from 60 diodes on each assembly. The same dewar, test parameters, and test station were used for each assembly during the thermal cycle/testing sequence as shown in Table 4-2 to eliminate any possible variables introduced from either the dewar or test station.

Table 4-2. Testing Parameters Used for I-Vs

Assembly	Dewar	Test Set	Window	Temperature
6537	22879	HP9826	ZnSe	120K
6131	22880	HP9826	ZnSe	120K
6508	22879	HP9826	ZnSe	120K
6146	3498	HP9836	ZnSe	120K
6509	3498	HP9836	ZnSe	120K

The test parameters used for I-V testing were zero field of view, 120K, zero bias, and zero background flux. I-Vs were taken at the beginning of this study, after 25 thermal cycles, and after 200 thermal cycles. The test history is shown in Table 4-3.

Table 4-3. Thermal Cycle and I-V History for Each Assembly

Assembly	1st I-V Test	Thermal Cycle	2nd I-V Test	Thermal Cycle	3rd I-V Test	Total Cycles
6537	X		X		X	3
6131	X	23	X			25
6508	X	23	X			25
6146	X	23	X	174	X	200
6509	X	23	X	174	X	200

After examining the I-V data, individual diode pixels were selected for detailed material analysis based on the changes in R_{QA} , R_{TA} , or change in the I-V curve. Typical I-V curves and variations in R_{QA} are shown in Appendix B. The particular diodes chosen for each hybrid are listed in Appendix C.

Assembly 6537 was established as the control hybrid, and more diodes were analyzed on that hybrid than the other four; 5 diodes were studied on the control sample to define "normal" variations and material irregularities not associated with thermal cycle stress. Forty-six "unusual" diodes were analyzed with the SEM from the results of 300 diodes analyzed with I-V characteristics.

4.3.2 Material Characterization Techniques

Failure analysis for the five hybrids was performed after a designated number of thermal cycles, and the data from the thermal cycled hybrids was compared to data from the control hybrid (Assy 6537).

Data collected on these hybrids included:

1. Evaluation of 60 diodes on each hybrid (See Appendix C for examples)
2. Pull test force
3. SEM analysis of passivation layer, indium bumps, interconnect metals
4. Dislocation revealing etch
5. SEM analysis of dislocations
6. X-ray double crystal rocking curve analysis

4.3.2.1 Pull-test (Tensile) Force

Pull testing is performed using a Sebastian III Pull Tester. The pull-test results are shown in Table 4-4.

Table 4-4. Hybrid and Pull (Tensile) Force for Each Assembly

Assembly	Thermal Cycles	Hybrid Force (lbs)	Pull Force (lbs)
6537	3	8.2	11.2
6131	25	8.1	0.5
6508	25	6.5	7.7
6146	200	5.0	5.8
6509	200	8.2	6.9

The pull force in assembly 6131 was unusually low, and was eliminated from further studies. The other pull test data showed pull strengths comparable to hybridization pressure, indicating good interconnect integrity. This was verified by inspecting the SEM pictures. Unlike previous studies, indium-to-indium weld reliability was not a limiting experimental factor.

4.3.2.2 Initial SEM Analysis

SEM analysis of the passivation layer, indium bumps, and interconnect metals of each designated diode and corresponding fanout unit cell was performed. Some examples are shown in Appendix D.

SEM analysis showed no surface degradation with thermal cycling. In addition, the analysis showed good indium welds in almost all parts of every hybrid. There were two unusual diodes -- assembly 6131 showed evidence of damage associated with electrostatic discharge or other catastrophic failure. Appendix E contains additional comments.

4.3.2.3 Dislocation Revealing Etch

The dislocation etch did not reveal a significant difference in dislocation density between control diodes and degraded diodes as was hoped, but the results were affected by the etchants for the removal of palladium contacts. The etch pits varied from hybrid to hybrid without correlation to thermal stress. The dislocation etch was an appropriately sensitive diagnostic technique, however, as shown in the test samples in Appendix A.

Some dislocation differences were noted in the nonhybridized arrays and the hybridized arrays. The dislocation etch morphologies between the two were different, suggesting that either hybridization and/or thermal cycling altered the material under the mesa. Conclusive results are difficult, however, due to the problems encountered with the palladium etchant. Both etchants etched the underlying HgCdTe more than expected. Pictures of test samples with the palladium

etches are shown in Appendix E. Pictures of the hybrids after palladium and dislocation etches are shown in Appendix F.

Large fissure-like cracks were seen on assembly 6509 (200 thermal cycles) before the dislocation etch, as shown in Figure 4-2. This suggests damage induced by hybridization or thermal cycling, but will need verification with a larger number of samples. It is also possible that the cracks were induced during tensile force testing.

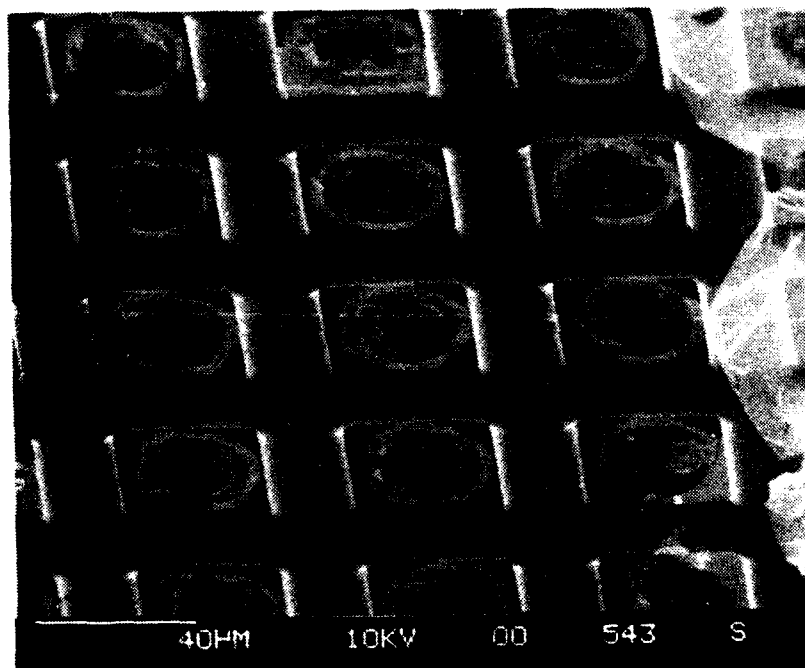


Figure 4-2. Cracks Appeared in Assembly 6509 Even Before Dislocation Etch (Post Pd etch, no SiO₂)

4.3.2.4 X-ray Rocking Analysis

X-ray rocking analysis is a noncontact technique in which the substrate is placed vertically onto a holder and the holder is rotated. A monochromatic beam of CuK α_1 X-rays is incident on the sample and the intensity of the diffracted X-rays is measured as the substrate is rotated about the Bragg angle. A plot of the X-ray intensity versus rotation angle is called a rocking curve. A measure of the crystal perfection is the full-width at half maximum (FWHM) of the X-ray rocking curve; a smaller FWHM is indicative of better crystalline quality.

Analysis was performed on four parts after thermal cycling. The results of analysis are shown in Appendix G. No correlation could be made between the number of thermal cycles and substrate degradation. The best quality material, as measured by rocking curves, was assembly 6509, that had been cycled 200 times.

The resolution and sensitivity of this analysis is limited. The graphs show general characteristic of the substrate, not of individual mesa areas. Computer-aided rocking-curve analysis (CARCA), a similar analysis tool with better resolution, could be used to evaluate individual mesa structures.

4.4 CONCLUSIONS AND RECOMMENDATIONS

4.4.1 Conclusions

1. A change in diode performance was induced by thermal cycle stress
2. The dislocation revealing etch was verified as a diagnostic tool
3. Removing palladium (the contact metal) was a severe obstacle for this study. Two different solutions were tried, each with limited success. Palladium adheres very well to HgCdTe, and removal damaged the underlying HgCdTe, adding some uncertainty to material diagnostics.
4. This study showed correlation between material properties and electrical degradation of individual diodes, but the results were shadowed by difficulties associated with removal of palladium contacts. The study provides a basis for more in-depth study, based on a detailed mapping and analysis technique, to further define and characterize the correlation of electrical performance with material properties.

4.4.2 Recommendations

1. A further, more detailed study should include hybrids without palladium contacts, readily available in pilot line samples.
2. The indium bumps should be removed chemically rather than mechanically, in order to distinguish between hybridization induced damage and de-hybridization (tensile) induced damage. (The effects of hybridization pressure on material integrity can be characterized by hybridizing detectors arrays to a flat, nonsticking surface. Although no electrical data of the diodes can be obtained with this analysis, the material properties may be observed with SEM and X-ray analysis.)
3. Other techniques appropriate in a more detailed analysis include computer-aided rocking-curve analysis (CARCA), transmission electron microscopy (TEM) with beveled etched samples, evaluation of dislocation depths, and investigation of material properties on alternative hybrid architectures.

Section 5

EFFECTS OF STRESS ON HFPA RELIABILITY

5.1 INTRODUCTION

The primary objective of this work was to evaluate the possible occurrence of damage induced in HgCdTe detector assemblies by hybridization and/or thermal cycling. The work conducted was divided into three tasks, the first of which entailed an investigation of the relationship between increased etch pit densities and degraded detector I-V characteristics. In the second task, attention was focused on determining the correlation between hybridization pressure and detector damage induced by hybridization. Work in the third task concentrated on evaluating the relationship between possible damage caused by thermal cycles and the number of thermal cycles seen by an array.

When sufficiently high stress is seen by HgCdTe material, damage will occur. The damage will result in a degradation of detector electrical performance and will increase the number of dislocations in the material. The extent to which the damage has caused electrical performance degradation can be determined by comparing the I-V characteristic of a set of diodes before and after the damage occurs. If the damage is localized, the I-V characteristics of diodes in the area of damage can also be compared with the I-V characteristics of diodes in undamaged or less damaged areas. A second method of evaluating the severity of the damage is to compare the densities of dislocations in damaged and undamaged material. The dislocation density can be analyzed using the SEM after appropriate dislocation-revealing etches have been applied.

The relationship between electrical performance degradation and increased etch-pit densities was studied in the first task. Damage was manually induced in several selected locations of a single array. An array was hybridized using standard hybridization parameters to a silicon fanout. The assembly was mounted in a flat pack on an 80 mil silica shim and wire bonded. IV testing was conducted. Tensile testing was performed and SEM photos of the fanout and detector were taken. Dislocations were revealed with appropriate etches and SEM photos of the detector were taken.

Hybridization is potentially a major source of stress that could result in detector damage. During hybridization of large-area HgCdTe detector arrays to silicon readouts, a certain amount of force is required to provide adequate indium cold welds. The stress seen by the diodes as a result of the hybridization force can be approximated by dividing the applied hybridization force by the total cross-sectional area of the indium bumps. At sufficiently high stress levels, diode damage can occur.

Three terms, hybridization force, hybridization pressure, and hybridization stress, are routinely used to quantify the magnitude of a particular hybridization. The most commonly used term, hybridization force, (sometimes improperly referred to as hybridization pressure) is the measured force used during hybridization. Hybridization pressure is a calculated quantity that is sometimes used to compare hybridizations of different detector configurations. It is calculated by dividing the hybridization force by the total cross-sectional area of the indium bumps in their undeformed state. As hybridization force is applied, the indium bumps cold flow and as a result the cross-sectional area of the bumps increases with increased force. The stress calculated by dividing the applied force by the resulting cross-sectional area is referred to as hybridization stress.

Twelve arrays were hybridized to silicon blanks at pressures ranging from 0 to 35 lb. Open dish probe techniques were used to measure I-V characteristics of several diodes from each array before and after hybridization. Two additional arrays, referred to as the wedged arrays, were hybridized with a 0 to 120 lb force gradient across the array. SEM analysis was used to evaluate the hybridizations. Metals were removed and the dislocation revealing etch was performed and SEM analysis was conducted on each array.

A second cause of stress that might cause diode damage is thermal cycling. When hybrids are taken from room to cryogenic temperatures (300K to 80K) the detector and the readout, to which the detector is attached, will contract. Due to the difference in the coefficients of thermal expansion of the HgCdTe detector and the silicon readout they will contract at different rates when cooled. The differential contraction will be taken up by the indium and will cause the indium to be stressed (especially at the edges and corners of the detector assembly). The stress will also be seen by the diodes at the indium-diode contact surface. The stress seen by the diodes will be alternating from the maximum to zero with each thermal cycle. If the alternating stress is large enough or if the stress is cycled enough times, diode damage can occur.

Eight detectors were hybridized to silicon fanouts using standard hybridization parameters (8.5 lb). After hybridization to fanouts six of the eight assemblies were mounted in flat packs on 80 mil silica shims and wire bonded. I-V testing was conducted on each after 100 and 200 thermal cycles. After 200 thermal cycles and final testing the assemblies were tensile tested (pull tested). SEM photos were taken of the detectors and the fanouts. The metals and passivation were removed from each detector with the appropriate solutions and a dislocation revealing etch was performed. The detectors were analyzed with the SEM and photos were taken.

Previous work (Section 4) has shown that by using the appropriate etches to remove detector metals and an additional etch to remove damaged HgCdTe that etch pits resulting from induced damage are revealed. Undamaged HgCdTe wafers generally have a background etch pit density

between 1×10^5 and 1×10^6 etch pits per square centimeter. 128^2 detectors with $50 \mu\text{m}$ center-to-center diode spacing have a diode area (unit cell) of $1 \times 10^{-5} \text{ cm}^2$ which equates to between one and ten etch pits per unit cell.

The work was conducted using large-area (128×128 diodes) long wavelength infrared HgCdTe staring arrays from 1987 assets. Arrays were hybridized to silicon fanouts in the first and third task and to silicon blanks in the second task. The array and fanouts were fabricated with $5 \mu\text{m}$ diameter by $12 \mu\text{m}$ tall cylindrical indium bumps on $50 \mu\text{m}$ centers. The fanouts test structures when hybridized to detector arrays provide electrical access to 128 of the 16,000 detector diodes on a 128^2 array. The task two arrays were hybridized to silicon blanks. The silicon blanks were fabricated specifically for use in the task to effort by dicing 20 mil thick silicon to a size slightly larger than the arrays used. Silicon blanks were used so that, when removed from the detectors after hybridization, electrical performance test procedures identical to those used before hybridization could be used. Silicon blanks were used in Task 2, because they could be easily removed from the array, allowing identical electrical tests to be conducted before and after hybridization.

5.2 EVALUATION OF RELATIONSHIP BETWEEN DISLOCATION ETCH PIT DENSITY AND I-V CHARACTERISTICS

5.2.1 Manually Induced Damage

A single array was intentionally damaged prior to hybridization using a sharp metal tipped probe. Several selected areas of the array were damaged. The damaged areas were carefully located at distances varying from one to five diodes from diodes accessed by fanout leads. The visible damage was restricted as much as possible to single diodes.

5.2.2 Hybridization

The array was hybridized to a silicon fanout. The assembly was hybridized at approximately 8.5 lb using standard hybridization techniques on a state-of-the-art computer interfaced hybridization machine.

After hybridization the assembly was mounted in a flat pack (68 pin leadless carrier) on a 80 mil silica shim. The flat pack and shim were used to facilitate testing and thermal cycling. Selected fanout lead lines from 66 of the 128 accessed diodes and two grounds were then wire bonded to the 68 flatpack contacts.

5.2.3 Electrical Testing

The I-V characteristics of the detector-fanout assembly were tested after hybridization using an automated I-V test station. Use of the automated test station was facilitated by the 68 pin flat-pack. The 66 diodes accessed via the flatpack and fanout were tested at 77K. Tests were done at zero field-of-view (0 FOV) and f/2. Test results included I-V curves, R_0A values, and R_fA values at -20 mV and -50 mV for each of the 66 tested diodes.

5.2.4 Cold-weld Evaluation

The array was tensile tested (pull tested) providing cold weld strength information and allowing for SEM analysis of the cold welds. A general survey of the indium on the array and on the fanout was conducted using the SEM. Photo micrographs were taken of each of the intentionally damaged areas, the four corners, the array center and any unusual areas.

5.2.5 SEM Etch-pit Analysis

The metals and the passivation layer were removed from the array with appropriate etches. The indium bumps were removed by immersion in hydrochloric acid (HCl) for five minutes. The molybdenum contact metal was removed with a 1:1:2 solution of HCl, hydrogen peroxide, and water. The array was agitated in the solution for two minutes. The SiO_2 passivation layer was removed using "BOE 500," a buffered hydrofluoric acid solution, for 45 sec.

Dislocations were revealed using a solution of hydrogen peroxide and ammonium hydroxide in a 2:1 ratio. The etch was performed for 8 minutes and the solution was not agitated.

The SEM was used to analyze the etch pit densities of various areas of the array. A general survey of the array was made and photomicrographs were taken of each of the four corners, the central area of the chip. Photomicrographs were also taken of each the intentionally damaged areas.

5.3 EVALUATION OF CORRELATION BETWEEN HYBRIDIZATION PRESSURE AND DETECTOR DIODE DAMAGE

5.3.1 Hybridization

The detectors were hybridized at various forces to silicon blanks. Hybridizations were done with the computer interfaced hybridization machine using standard techniques. The arrays were hybridized at forces that ranged from 0.0 lb to approximately 35 lb. The selected forces were multiples (0, 1/2, 1, 2, 4) of 8.5 lb, the standard hybridization force for 128² arrays.

Two partial arrays were also hybridized to silicon blanks. They were hybridized so that a stress gradient was seen across the chip. No contact was made in one corner of each partial array, resulting in zero stress in those corners. In the opposite corners, the induced stress was approximated as that caused by hybridization of a 128^2 array at 120 lb (15 times standard hybridization force).

Silicon was used so that the hybrids could be disassembled after hybridization without introducing additional stresses to the detector. Hybrid disassembly was required so that the same testing procedures could be used to evaluate the I-V characteristic of the detectors before and after hybridization and to allow etch pit analysis to be conducted.

5.3.2 Electrical Testing

The I-V characteristics of the arrays were tested before and after hybridization using a manual probe station. The detectors were submerged in LN_2 and 21 diodes were probed under a microscope with a 2 mil gold wire.

One set of five arrays was tested with an open field-of-view. I-V curves were plotted for each of the 21 probed diodes and R_T values at -150 mV and R_0 values were calculated manually for the first five tested diodes of each array.

A second set of four detectors was also probed manually but was tested at zero field-of-view and data was taken using an automatic data acquisition equipment. The automated equipment used had an auto-scaling capability which allowed for a more accurate evaluation of I-V characteristics. The data generated included I-V curves, R_0 values, and R_T values at -20 mV and -50 mV for each of the 21 probed diodes.

5.3.3 Indium Squeeze-out Evaluation

The indium squeeze-out of each of the hybridized arrays was evaluated using the scanning electron microscope (SEM). A general survey of each array was made. Particular attention was given to the amount of squeeze-out in various areas and to the squeeze-out uniformity across the chip. Photomicrographs were taken of all unusual damage and of the areas near the four corners and the center of each detector.

5.3.4 SEM Etch-pit Analysis

SEM analysis was performed to determine the etch pit densities of various areas of the array. A general survey of each array was made and photomicrographs were taken of each of the four corners, the central area of the chip.

5.4 EVALUATION OF CORRELATION BETWEEN THERMAL CYCLES AND DETECTOR DIODE DAMAGE

5.4.1 Hybridization

Detectors were hybridized to silicon fanouts. The hybrids were assembled at approximately 8.5 lb using standard hybridization techniques. Hybridizations were made using a computer interfaced hybridization machine.

After hybridization the assembly was mounted in a flat pack (68 pin leadless carrier) on a 80 mil silica shim. The flat pack and shim were used to facilitate testing and thermal cycling. Selected fanout lead lines from 66 of the 128 accessed diodes and two grounds were then wire bonded to the 68 flat pack contacts.

5.4.2 Electrical Testing

The current-voltage (I-V) characteristics of the detector-fanout assemblies were tested after hybridization using an automated I.V. test station. The 66 diodes accessed via the flatpack and fanout were tested at 77K. Tests were done at zero field-of-view (0FOV) and f/2. Test results included I-V. curves, R_0A values, and $R_T A$ values at -20 mV and -50 mV for each of the 66 tested diodes. Testing was repeated on each of the assemblies.

5.4.3 Cold-weld Evaluation

The arrays were tensile-tested (pull-tested) providing cold weld strength information and allowing for SEM analysis of the cold welds. A general survey of the indium on each array and on each fanout was conducted using the SEM. Photo micrographs were taken of each of any unusual damage, and of the areas near the four corners and the center of the array.

5.4.4 SEM Etch-pit Analysis

The metals were removed using the same method described earlier. The CdTe passivation layer was removed using a proprietary process. Dislocations were revealed using the previously mentioned etch procedure.

The etch-pit density of each of the arrays was analyzed with the SEM. A general survey was made and photomicrographs were taken.

5.5 ETCH-PIT DENSITY AND ELECTRICAL PERFORMANCE OF MANUALLY DAMAGED ARRAYS

5.5.1 Increased Etch-pit Density near Induced Damage

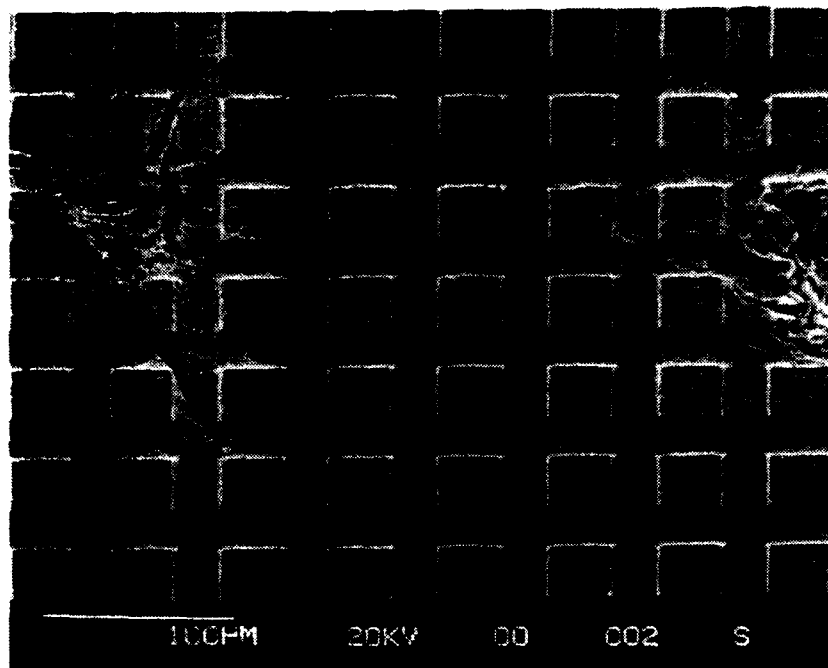
Testing and SEM analysis of the manually damaged Task 1 IRFPA demonstrated that increased dislocation densities and degraded electrical performance results when HgCdTe detector material is damaged. Dislocations were measured as revealed etch pits using SEM analysis. Two SEM photographs, taken of the IRFPA after application of the dislocation revealing etch, are shown in Figure 5-1. The first photo, Figure 5-1a, shows the etch pit density typical of areas near induced damage. Etch pit densities typical of areas remote from induced damage are shown in Figure 5-1b.

The two photographs in Figure 5-1 along with the remainder of the SEM analysis showed that the density of revealed dislocation increases dramatically in the immediate area near material damage. A point of induced damage is located in the upper left-hand corner of Figure 5-1a. The increased density of etch pits in the immediate area is visually obvious. The high density of revealed dislocations in the upper right-hand corner of Figure 5-1a is due to a second point of induced damage located just outside of the photographed area. The localized nature of the increased etch pit density near the damage can be seen by comparing the density four or more diodes away from the point of induced damage to that of diodes in remote locations (Figure 5-1b).

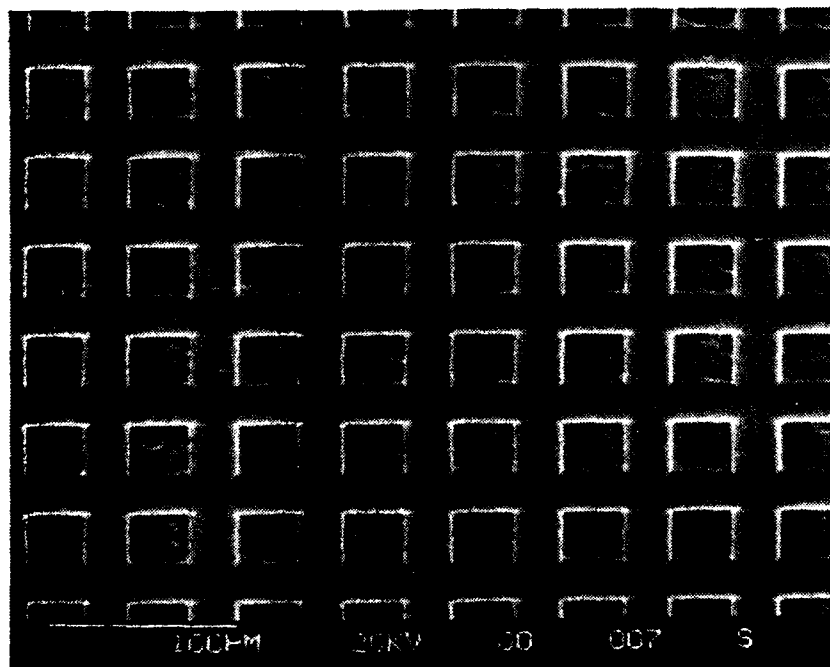
5.5.2 Degraded Electrical Performance near Induced Damage

Electrical testing revealed that performance of diodes near induced damage was significantly lower than for remote diodes. The 11 numbered diodes shown in Figure 5-1 were among those diodes accessed electrically through the fanout, to which the array was hybridized. The I-V curves of the nine numbered diodes shown in Figure 5-1a are plotted in Figure 5-2a. The two numbered diodes pictured in Figure 5-1b and seven additional diodes from areas isolated from induced damage have their I-V curves plotted in Figure 5-2b.

The degradation in I-V characteristics of diodes near points of induced damage can be seen by comparing the curves in Figure 5-2a to those in Figure 5-2b. Two quantities that decrease with degraded electrical performance are R_0 , the resistance at zero voltage, and R_T at -50 mV. Decreased R_0 of the damaged diode is seen as an increased I-V curve slope at the origin and decreased R_T can be seen as increased slope at -50 mV. One additional visual indication of reduced performance is reverse bias breakdown of the curves plotted in Figure 5-2a. The two linear I-V curves, diodes 10 and 17, indicate shorts. From Figure 5-1a it shows that diode 10

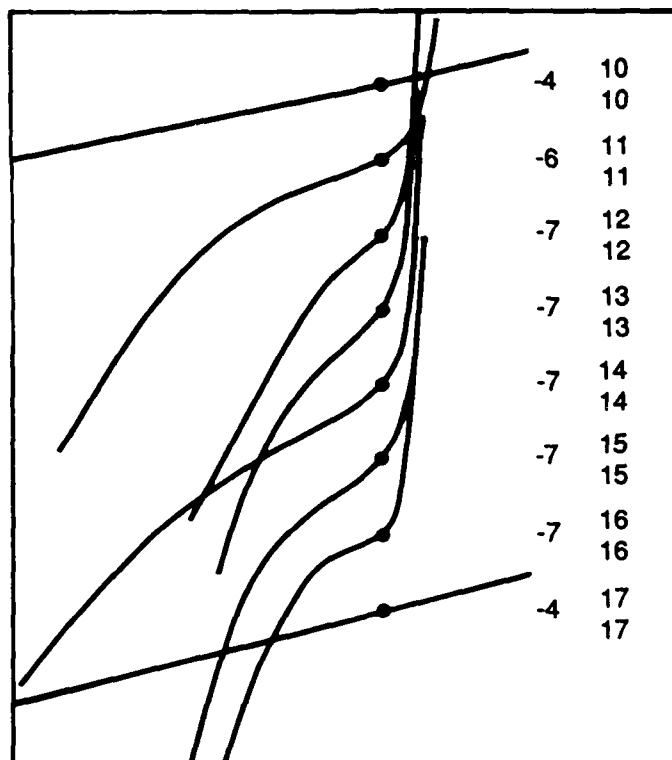


(a) Near Induced Damage

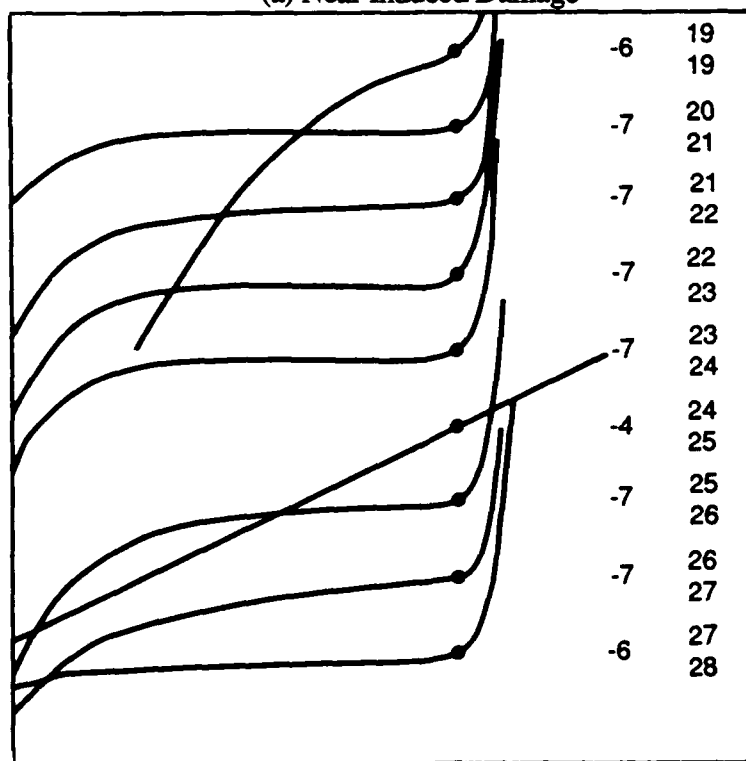


(b) Remote from Induced Damage

Figure 5-1. Increased Etch-pit Density near Induced Damage. The dramatic increased in the density of revealed dislocations can be seen by comparing the densities near and remote from damage.



(a) Near Induced Damage



(b) Remote from Induced Damage

Figure 5-2. Degraded Electrical Performance near Manually Induced Damage. Degradation of electrical performance of diodes near induced damage can be seen as increased slope at 0 mV and -50 mV when compared to diodes remote from damage.

is the diode closest to the point of induced damage and with the highest density of etch pits and diode 17 is the closest diode to a material fracture. Both of these shorts are thus explained by the proximity of the diodes to points of damage.

5.5.3 Increased Etch-pit Density and Degraded Electrical Performance Correlation

Direct correlation between increased dislocation density, caused by intentional damage, and degraded electrical performance was demonstrated by a comparison of etch-pit density and I-V characteristics of various diodes. Compiled in Table 5-1 are the etch pit densities, (cm^{-2}) and etch pits per unit cell, R_0 , and R_T at -50 mV for the 18 diodes thus far discussed. The first 9 diodes, those from the area near damage (pictured in Figure 5-1a), are tabulated in order of increasing distance from the point of induced damage. The correlation between decreased etch pit density and the improved electrical performance with increased distance can be seen from the tabulated values of diodes 1 through 9. The statistical equivalence of the data from last nine diodes indicates that the densities and performance of these diodes are unaffected by the remote damage. Diode 15 was at a distance of only 7 diodes from a point of induced damage, demonstrating the localized nature of induced damage discussed in section 5.5.1.

The sensitivity of the methods used to analyze etch pit densities and to measure electrical performance to damaged HgCdTe material was validated by the data taken at known points of manually induced damage. The correspondence of revealed etch pits to damage can be seen in Figure 5-1. The I-V curves shown in Figure 5-2 along with the electrical data from Table 5-1 demonstrate the correlation of performance data to areas of damage. Table 5-1 also shows the agreement of the two analysis/testing methods.

5.6 DIODE STRESS RESULTING FROM HYBRIDIZATION AT VARIOUS PRESSURES

5.6.1 Indium-bump-limited Hybridization Stress

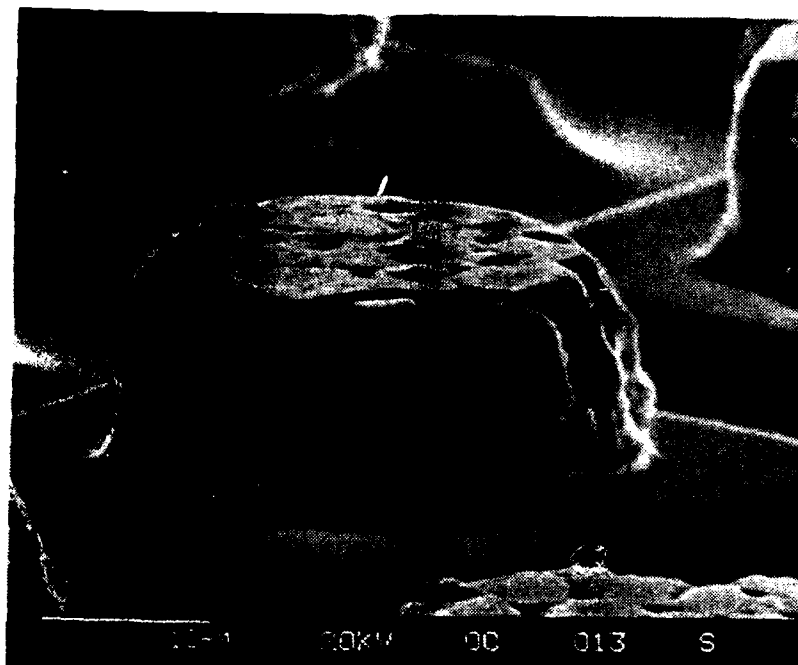
The stress seen by the IRFPA due to hybridization was found to be limited by the cold flow characteristics of indium bumps. Typically deformed bumps from two arrays, the first hybridized at 8.4 lb and the second at 34.1 lb, are pictured in Figures 5-3a and 5-3b respectively. These photos show that cross-sectional indium bump area is greatly increased by increased hybridization pressure. The stress seen by each of the diodes is calculated by dividing the hybridization force by the combined cross-sectional indium bump area of the array. Shown in Table 5-2 are hybridization force, average resulting bump diameter and area, total indium area and calculated hybridization stress for several of the arrays hybridized in Task 2. The calculated stresses effect is independent of hybridization force. The calculated stress limit corresponds well with tabulated values of indium tensile strength (500 psi).

Table 5-1. Correlation between Increase Etch Pit Density and Degraded I-V Characteristics Due to Intentionally Induced Damaged

	Distance from Damage Point (μm)	Etch Pit Density (cm^{-2})	Pits/Unit Cell	R_0	R_r at -50 mV
Damaged Diodes					
10	25	3×10^6	400	4.7×10^3	5.0×10^3
19	35	2×10^6	200	1.4×10^5	2.5×10^5
11	75	2×10^6	200	2.3×10^5	2.4×10^5
17	100	Fracture		7.5×10^3	4.1×10^3
13	100	5×10^3	50	9.2×10^3	8.3×10^5
12	125	1×10^6	80	9.2×10^3	6.8×10^5
16	140	5×10^5	50	1.3×10^6	8.5×10^5
14	155	3×10^5	25	9.2×10^5	1.8×10^6
15	180	1×10^5	10	9.5×10^5	1.2×10^6
Remote Diodes					
21	2000	2×10^4	1	3.3×10^6	7.7×10^7
22	1120	2×10^4	1	3.5×10^6	5.5×10^7
23	1700	2×10^4	1	1.2×10^6	1.5×10^8
24	2500	2×10^4	1	1.8×10^6	1.4×10^8
25		Fracture			
26	1250	2×10^4	1	2.7×10^6	3.9×10^7
27	1600	2×10^4	1	3.4×10^6	9.8×10^6
28	1600	2×10^4	1	0.2×10^6	2.5×10^6

5.6.2 Hybridization-induced Etch-pit Density

SEM analysis of the Task 2 IRFPAs revealed that increased etch pit densities occurred only where hybridization forces equal to or larger than 120 lb were applied. Etch pit densities typical of the arrays hybridized at pressures ranging 0.0 lb (unhybridized arrays) to 35 lb are presented in Figure 5-4. These arrays were hybridized at 8.4 lb (Figure 5-4a) and 35.1 lb, (Figure 5-4b) and the etch pit were densities found to be statistically equal to that of arrays that were not hybridized. The etch pit densities of the arrays pictured in Figure 5-4 as well as the remainder of Task 2 arrays hybridized with pressures up to 35 lb are compiled in Table 5-3. The tabulated results show that there is no change in etch pit density with increased pressure which corresponds well with the independence of stress and hybridization force discussed above.

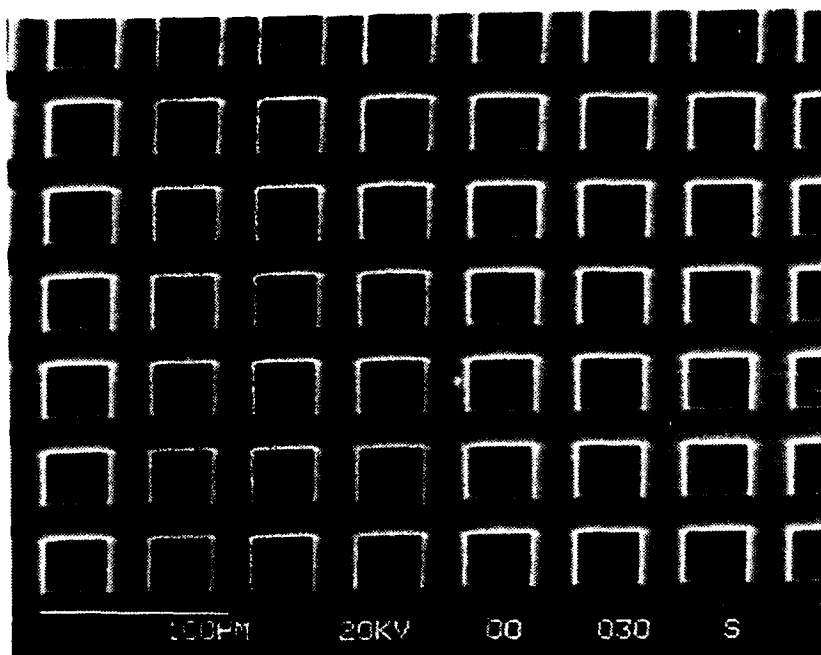


(a) Hybridized at 8.4 lb

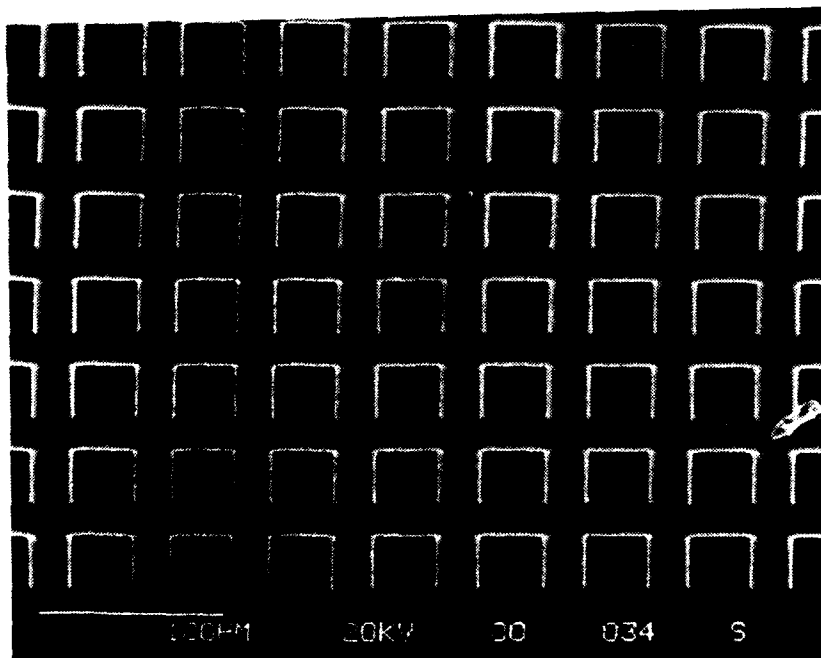


(b) Hybridized at 34.1 lb

Figure 5-3. Hybridization Stress Buffered by Cold Flow Characteristics at Indium Bumps. Stress Calculated by dividing applied force by resulting cross-sectional indium area does not increased with increased hybridization force.



(a) Hybridized at 8.4 lb



(b) Hybridized at 34.1 lb

Figure 5-4. Etch-pit Density Not Increased by Hybridization Forces between 0 and 120 lb. It can be seen that the density of revealed dislocations is unaffected by a four fold increase in hybridization force.

Table 5-2. IRFPA Stress Not Strongly Affected by Increased Hybridization Force

Hybridization Force (N)	Bump Diameter (μm)	Bump Area (μm^2)	Indium Area (cm^2)	Hybridization Stress
(4.7 lb)	~19	280	4.6×10^{-2}	660
(8.8 lb)	~23	420	6.8×10^{-1}	830
(17.1 lb)	~30	710	1.2×10^{-1}	950
(34.1 lb)	~34	910	1.5×10^{-1}	1500

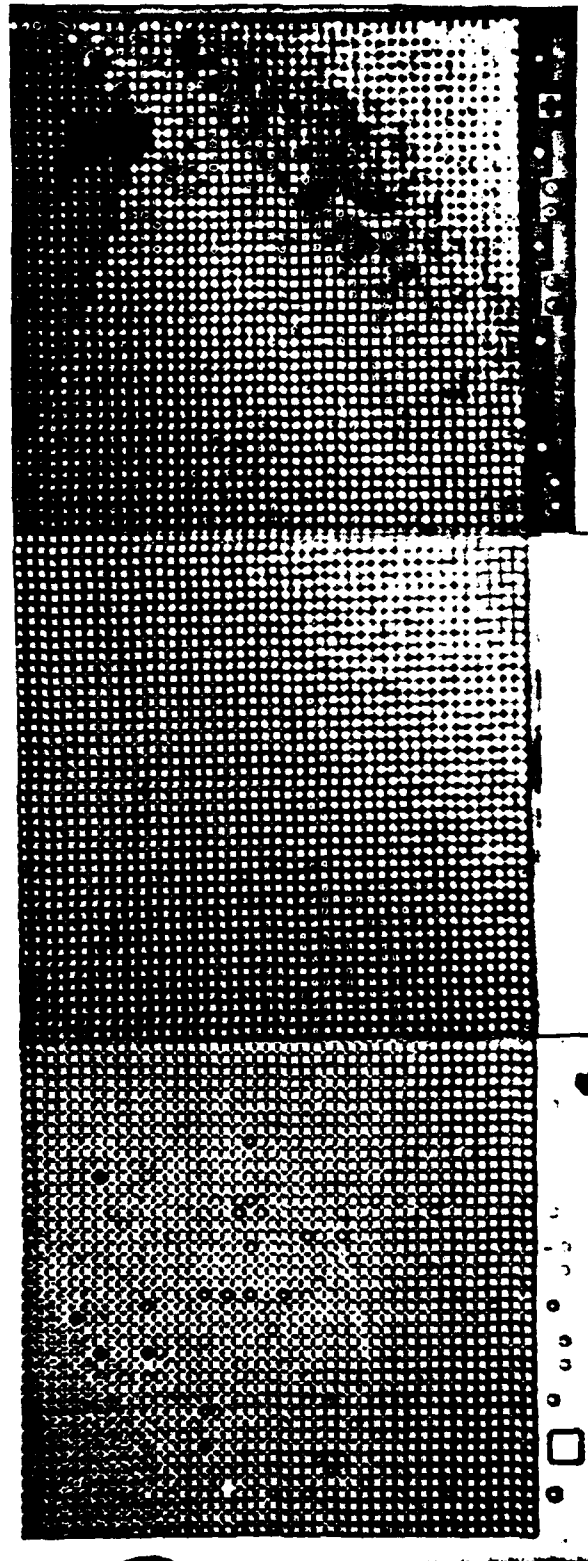
Equivalent hybridization forces in excess of 120 lb were reached in areas of two of the Task 2 IRFPAs. These extremely high, 15 times standard, hybridization forces were achieved by hybridizing the arrays with a force gradient across their diagonals. A set of photographs of one of the arrays taken before indium removal is presented in Figure 5-5. In Figure 5-5, indium squeeze out ranging from zero in the upper left-hand corner to a maximum in the lower right-hand corner can be seen. Zero squeeze-out was achieved by insuring that no contact was made in one corner. The indium squeeze out in the lower left-hand corner is so extreme, although difficult to see in Figure 5-5, that no indium remains on the top of the diode mesas.

Two SEM photomicrographs of the lower right-hand corner of the array pictured in Figure 5-5 taken after application of the dislocation revealing etch are shown in Figure 5-6. A "line" of demarcation (color change) can be seen in Figure 5-6a. Pictured in Figure 5-6b is a close-up along the "line" that shows that the color change is caused by a dramatic change in the density of revealed dislocations. In comparing Figure 5-5 and Figure 5-6, it can be seen that the "line" of demarcation occurs at the boundary where indium no longer remains on top of the mesas. Damage occurs only in the area where no indium remains to limit the stress seen by the HgCdTe material. This observation correlates well with the results discussed earlier that indicated that the cold flow characteristics of the indium bumps limit the stress seen by the IRFPA.

By comparing the indium squeeze out in various areas of the array pictured in Figure 5-5 to the squeeze out of arrays hybridized at known forces, such as those tabulated in Table 5-2, the equivalent hybridization force at several locations can be approximated. Assuming that the force gradient across the array is linear, it can be determined that the "line" of demarcation occurs at the 120 lb force "line".

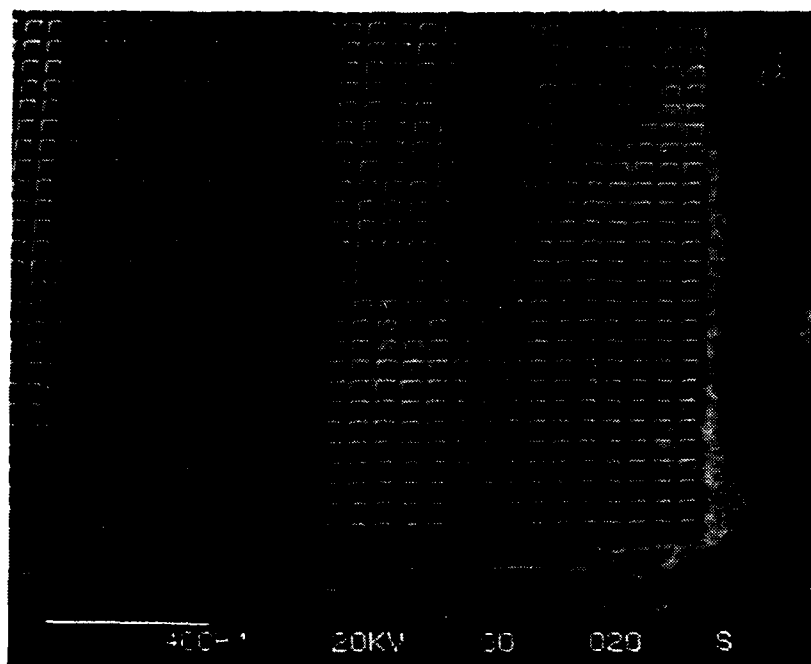
The observation that the etch pit density is increased only in areas where indium buffering does not exist is confirmed quantitatively in Table 5-3 where the pit densities and the equivalent hybridization force at several location across the array are tabulated. The two etch pit values at 120 lb are for the diodes immediately to the left and to the right of the "line" of demarcation. The density value listed for 0 lb was obtained from the corner of the array where no contact was made. The densities at points exposed to forces less than 120 lb show no significant increase from the density at 0 lb.

LOW FORCE

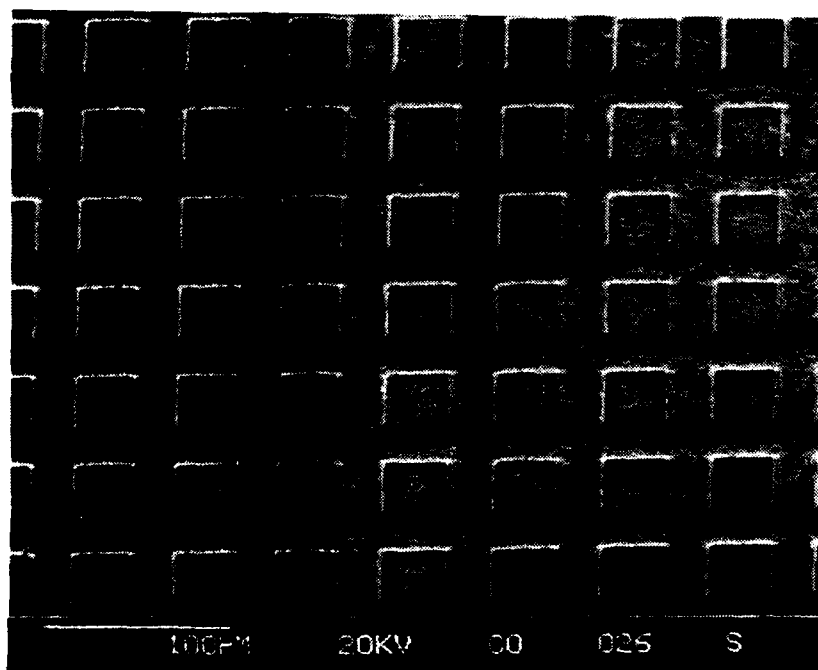


HIGH FORCE

Figure 5-5. Indium Squeeze-out Due to Hybridization Force Gradient. Hybridization force ranges from 0 lb in the upper left-hand corner to greater than 120 lb in the lower right-hand corner.



(a) Lower Right-Hand Corner



(b) Magnification Along "Line" of Demarcation

Figure 5-6. Increased Etch-pit Density Due to Hybridization a Force in Excess of 120 lb. A dramatic increase in the density at revealed dislocation can be seen to the right of the "line" of demarcation.

The data in Table 5-3 and the photos on Figure 5-6 also confirm the observation that increased etch pit densities are localized to the area of damage. In Figure 5-6b, it can be seen that the density of pits at a distance of greater than 3 or 4 diodes is at the level of the remainder of the undamaged portion of the array. The dramatic change in density at the 120 lb "line" seen shown in Table 5-3 also demonstrates the localized nature of increased etch pit density.

Table 5-3. Etch-pit Density Versus Hybridization Force

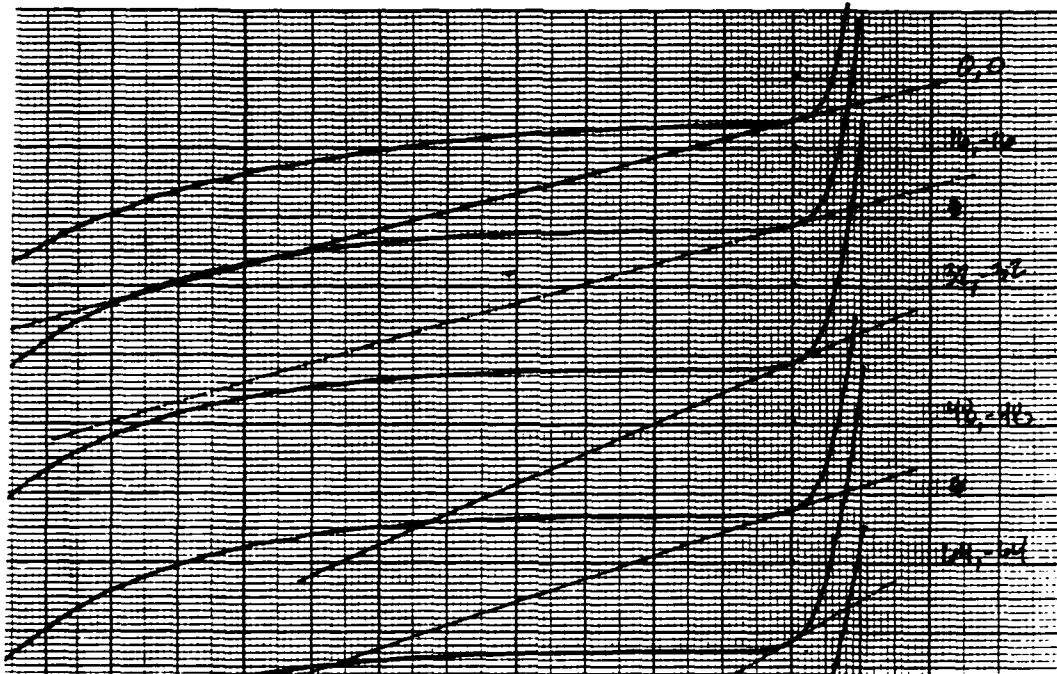
No.	Hybridization Force (lb)	Revealed Dislocation Density	
		(pits/wall)	(pits/cm ²)
23	4.7	3	1.1×10^5
10	8.8	2	4.3×10^4
19	8.8	2	6.3×10^4
21	8.8	2	4.1×10^4
20	17.5	6	2.4×10^5
15	34.1	2	3.5×10^4
16	34	2	5.5×10^4
22	34	2	4.4×10^4

5.6.3 Effects of Hybridization on Electrical Performance

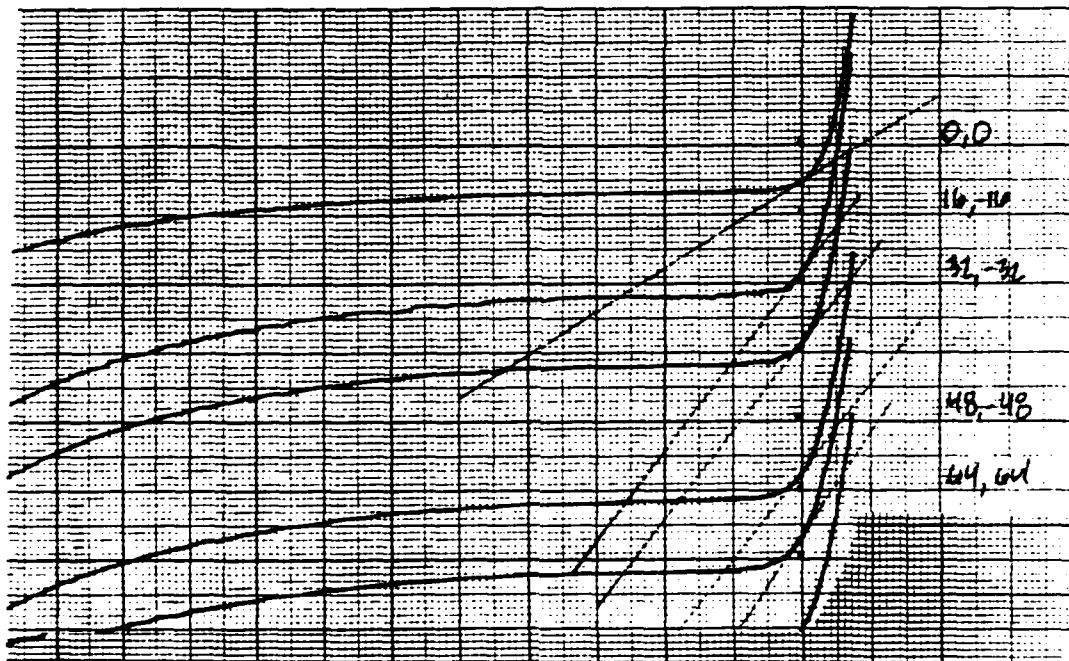
Electrical performance results correlated well with the etch pit results discussed in Section 5.6.2. No degradation in electrical performance due to hybridization at forces ranging from 0 to 35 lb occurred. However, difficulties involved in testing made the results inconclusive.

A 0.001-inch diameter gold wire was used to probe each selected diode. The indium bump to which electrical contact was made had a diameter of 0.0005-inches. It was very difficult to make good electrical contact between the gold wire and the selected bump without changing the probed bump and the adjacent bumps. As a result, the data was noisy. Significant degradation, however, such as that shown in Figure 5-2b would have been discernable.

I-V curves of several diodes from a Task 2 array hybridized at 34 lb are shown in Figure 5-7. The pictured array and several others were tested using open-dish probing. The I-V curves in Figure 5-7a were measured before hybridization and those in Figure 5-7b were generated after hybridization. A comparison of the two sets of I-V curves show that the I-V characteristics of the tested diodes are unchanged by hybridization. Indications of degradation such as early reverse bias breakdown or a change in slope at zero bias, R_0 , do not occur. The only consistent changes that occur is a shifting of the curves along both the current and voltage axis. These shifts



(a) Before Hybridization



(b) After Hybridization

Figure 5-7. Open-field-of-view Electrical Performance Unchanged by Hybridization at 35 lb. I-V curves typical of arrays viewing warm scene show no degradation due to hybridization.

do not however correlate to increase hybridization force and are, therefore, assumed to be artifacts of the test procedures.

Testing was also done with arrays looking at a cold scene, a 77K body (zero field of view). Before and after hybridization I-V curves are plotted in Figure 5-8a and Figure 5-8b for an array hybridization at 35 lb. As seen with the open dish probe results, no significant change in I-V characteristics due to hybridization occurs.

5.7 THERMAL CYCLING RESULTS

5.7.1 Etch-pit Density

SEM analysis of arrays being subjected to 200 thermal cycles showed no increase in etch pit density above HgCdTe background levels (1 to 10 per unit cell) as described Section 5. The etch pit densities after 200 thermal cycles were also no greater than levels observed on partial arrays that were not exposed to thermal cycling. Etch pit densities typical of arrays exposed to zero and 200 thermal cycling. Etch pit densities typical of arrays exposed to zero and 200 thermal cycles are presented in Figure 5-9a and Figure 5-9b respectively.

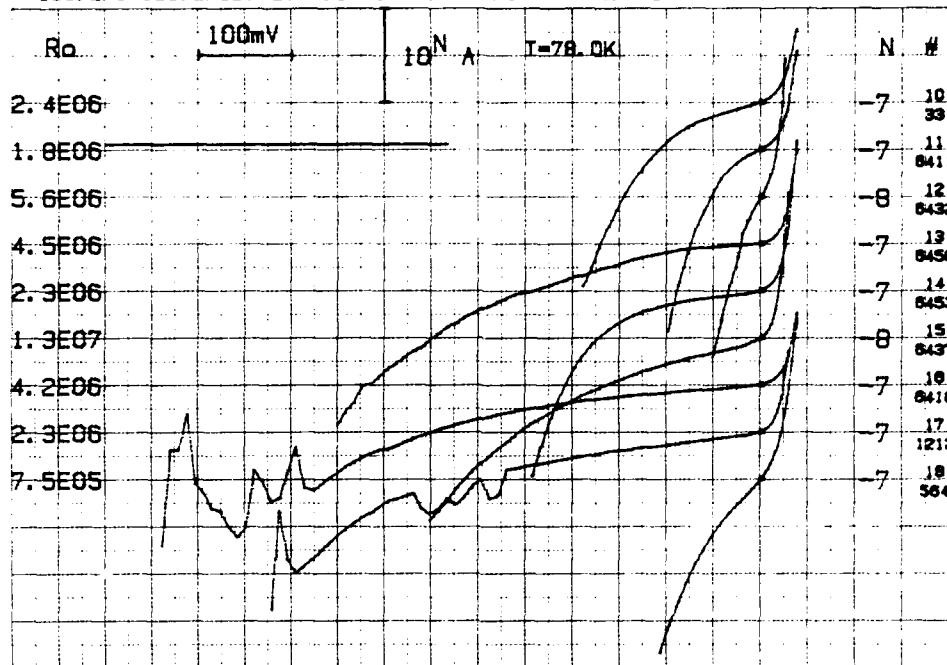
5.7.2 Electrical Performances

Table 5-4 summarizes R_0 and R_r at -50 mV values from an array prior to thermal cycling and after 100 and 200 thermal cycles. Table 5-4 shows that essentially no degradation in I-V characteristics was observed after 200 thermal cycles. More statistics are needed, however, to generalize this conclusion.

Table 5-4. Thermal Cycle Results

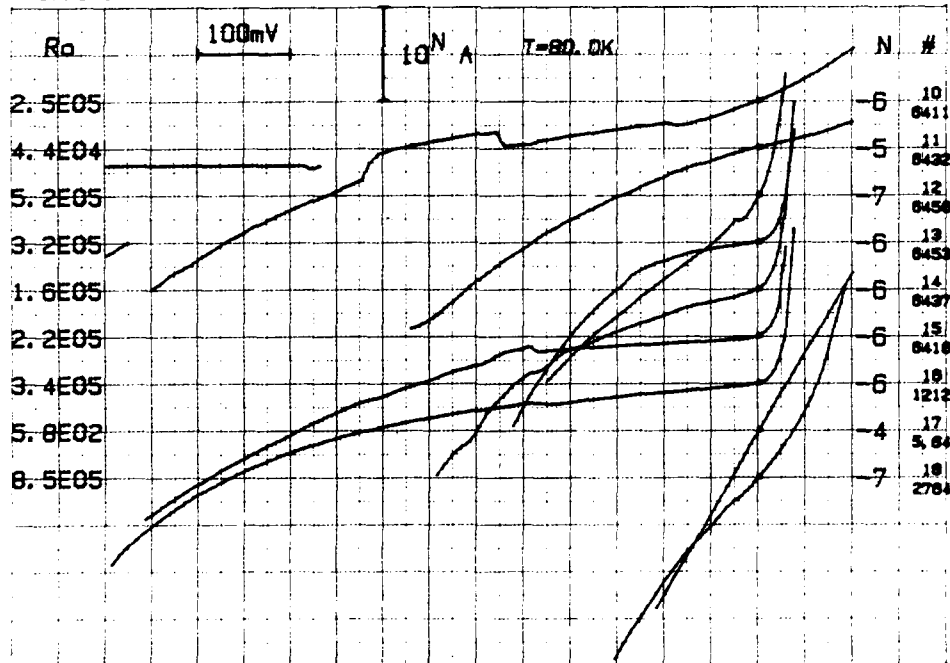
Assembly 67A	R_0	R_r at -50 mV
Before thermal cycling	9.8×10^5	4.5×10^5
After 100 thermal cycles	9.6×10^5	4.1×10^5
After 200 thermal cycles	9.6×10^5	3.6×10^5

V-839.2/I-803.2/CB1-Z9-7.2 SiO2 LOT1 #10 Qb=0.00e00 10-18-88



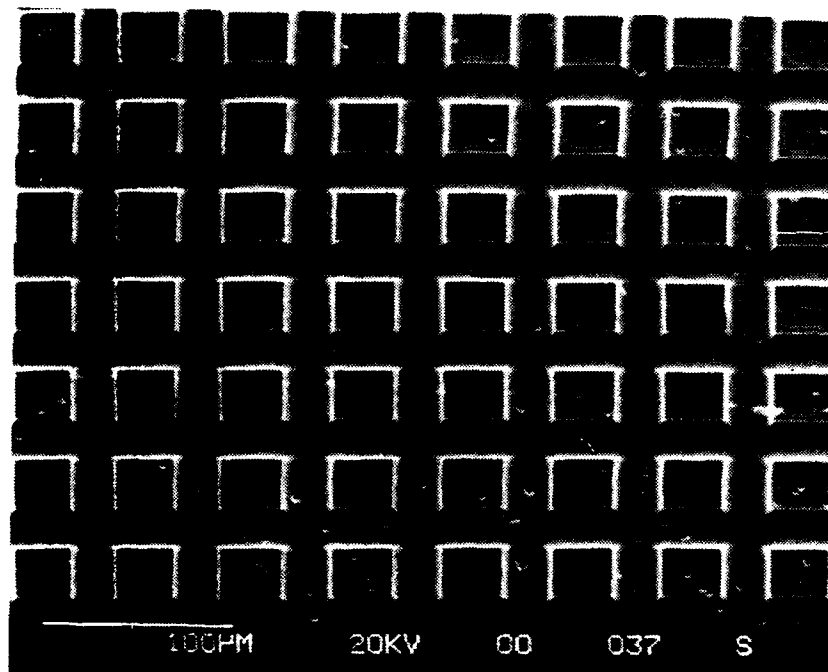
(a) Before Hybridization

V837.2/I803.2/CB1-Z9-7.2 #10 LOW BACKGROUND Qb=0.00e00 10-18-88

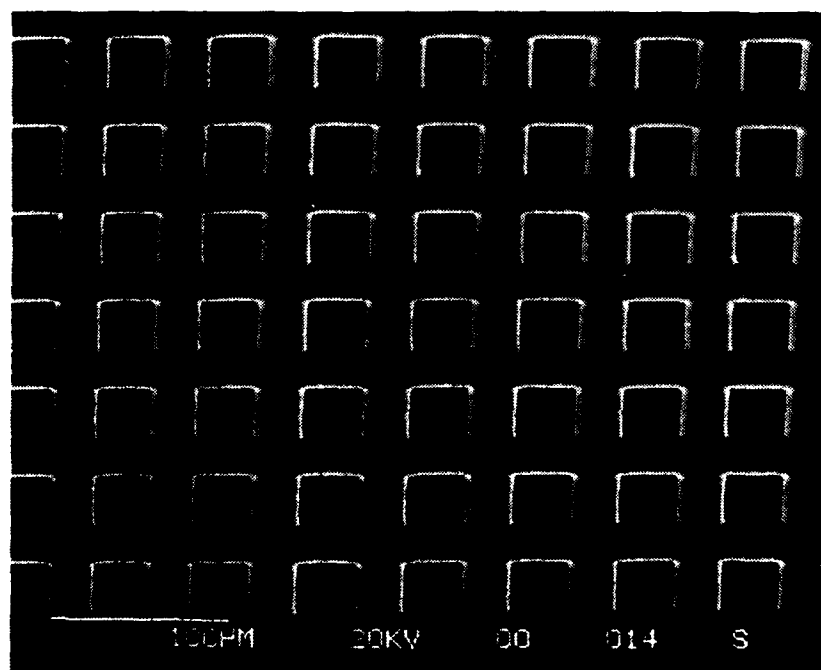


(b) After Hybridization

Figure 5-8. Zero Field-of-view Electrical Performance Unchanged by Hybridization at 35 lb. I-V curves typical of arrays viewing a cold scene show no degradation due to hybridization



(a) Without Thermal Cycling



(b) With 200 Thermal Cycles

Figure 5-9. Etch Pit Density Not Affected by 200 Thermal Cycles. It can be seen that no increase in revealed dislocations occur as a result of 200 thermal cycles.

5.8 CONCLUSIONS

Correlation was found between increased etch-pit density and degraded electrical performance resulting from intentionally damaged HgCdTe IRFPA detector material. Stress caused by hybridization of IRFPAs was prevented from reaching levels high enough to lead to HgCdTe material damage by the cold-flow characteristics of the indium bumps. The stress was limited to approximately 1000 psi up to a hybridization force of 120 lb, at which point a complete squeeze-out of the indium prevented buffering. Stress experienced by HgCdTe material due to up to 200 thermal cycles was also determined to be insufficient to cause increased etch-pit density or degraded electrical performance.

Section 6

SUMMARY AND CONCLUSIONS

6.1 INITIAL THERMAL CYCLE STUDY

An initial study was made to identify the failure modes associated with thermal cycling PV HgCdTe hybrid arrays. As a vehicle for this testing, a 160×3 (12) LWIR HgCdTe array hybridized to a Si readout was tested and thermal-cycled up to a cumulative total of 81 thermal cycles. The hybrid was then pulled apart and analyzed in the SEM. Two primary failure modes were identified:

1. Interconnect failure due to delamination at the contact metal/HgCdTe interface
2. Passivation delamination from the HgCdTe surface causing device degradation.

These failures were apparently due to unwanted surface contamination during the processing of this device and are not inherent limitations of hybrid detector arrays. These problems were eliminated in the process and did not affect further experiments.

6.2 INDIUM CREEP TESTING

Three lap shear specimens with pure indium as the bond material were tested to determine the creep properties of indium in shear, at three temperatures and three stress levels. Results show that the creep rate in indium increases with increasing test temperature and holding stress. The data determined in this study are in agreement with the data published by the National Bureau of Standards on indium. These results can be used for modeling of metallurgical processes in indium.

6.3 DIAGNOSTIC TECHNIQUE EVALUATION

The use of an etchant on HgCdTe to reveal changes in dislocation density as a result of hybridization and/or thermal cycling was verified, and procedures were developed for stripping of metallization and passivation layers on completed arrays and etching the HgCdTe to reveal etch pits. It was found that palladium contacts were difficult to remove and tended to cause anomalous etching characteristics, which made etch-pit density measurements difficult. X-ray rocking-curve measurements were briefly evaluated as a technique to characterize defects in the HgCdTe; results however, were inconclusive.

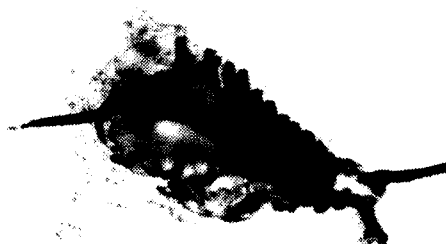
6.4 EFFECTS OF STRESS ON HFPA RELIABILITY

No degradation in the I-V characteristics or increase in the dislocation density was found for HgCdTe arrays thermal cycled from 300K to 77K for a total of 200 cumulative cycles. However, HgCdTe detector arrays were intentionally damaged specifically to evaluate the effect of an increase in dislocation density on the electrical properties of the diodes. A correlation was found between an increased etch-pit density and a degradation in HgCdTe detector I-V characteristics resulting from the intentional damage to the HgCdTe.

Detector damage caused by hybridization that would cause degraded diode performance is prevented by the stress-buffering nature of the indium bumps. The indium limits the stress seen by the diodes to approximately 1000 psi and, as a result, prevents damage and degradation. Damage is prevented for hybridization forces up to as large as 120 lb, at which point the indium is squeezed completely off the mesa and can no longer act as a stress buffer.

Appendix A
DISLOCATION ETCH MICROGRAPHS

Evaluating and optimizing the dislocation etch was conducted on scrap HgCdTe substrates from the same wafer as the five hybrids in this study.



(a)

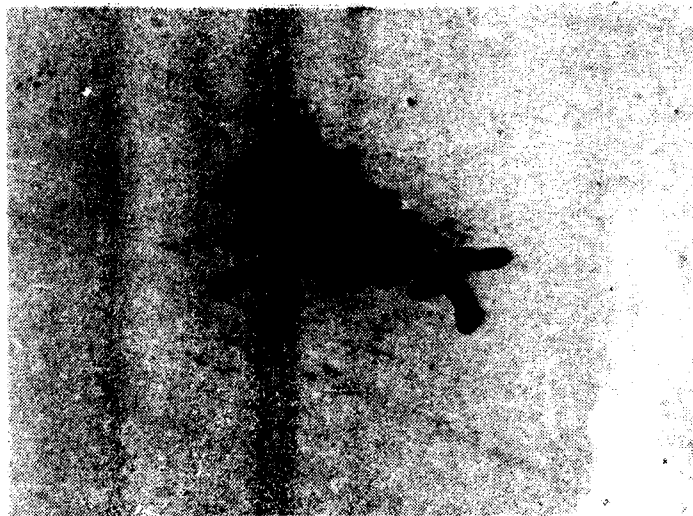


(b)

Micrographs of Etched Surface to Reveal Defects ($\text{H}_2\text{O}_2:\text{NH}_3\text{OH}$ 2:1, 5 min) (a) 500X, (b) 100X



(a)

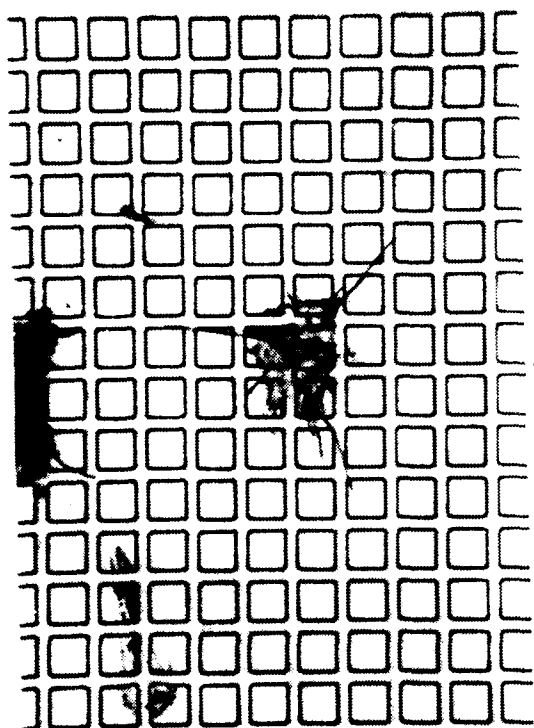


(b)

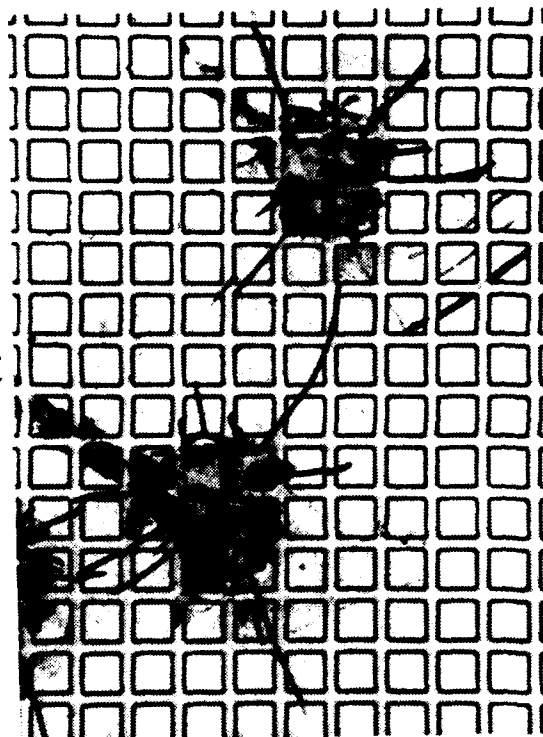


(c)

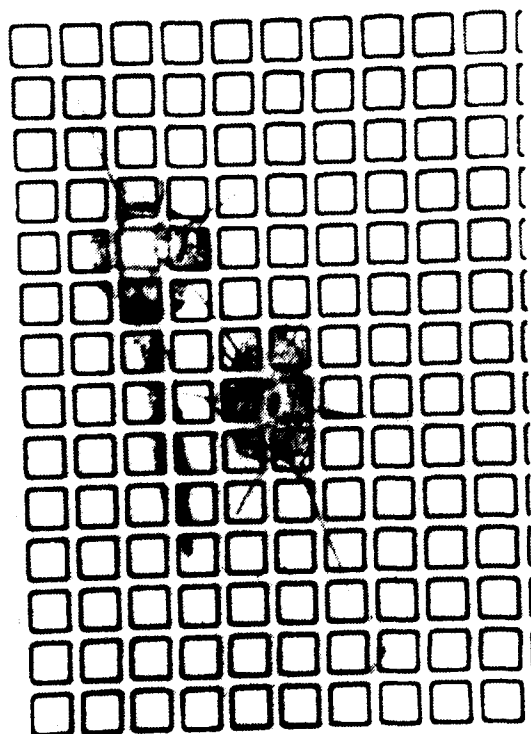
Micrographs of Etched HgCdTe Surface (500X) After Various Etch Times ($\text{H}_2\text{O}_2:\text{NH}_3\text{OH}$ 2:1,
(a) 10 min, (b) 15 min, and (c) 20 min.



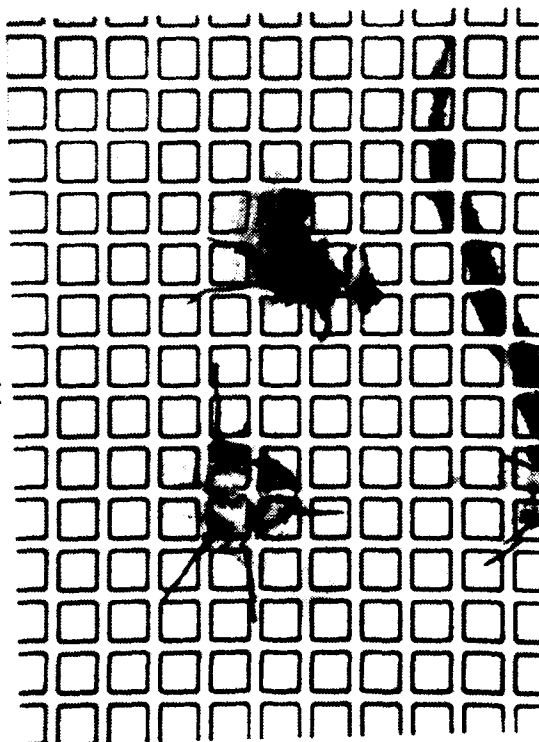
(b)



(d)

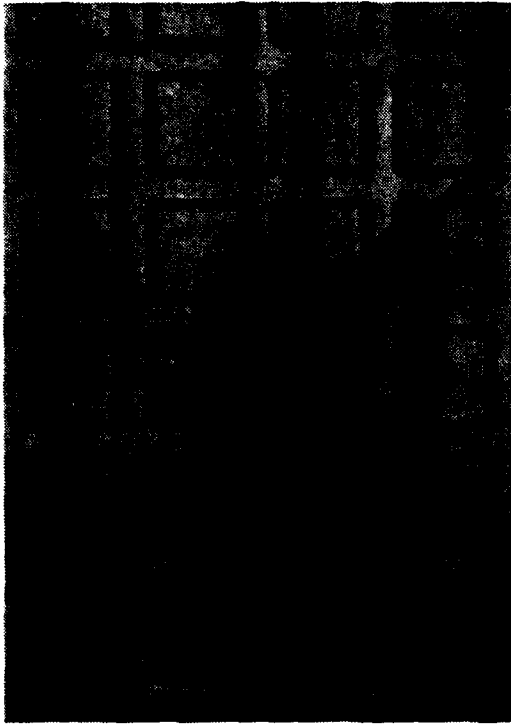


(c)



(b)

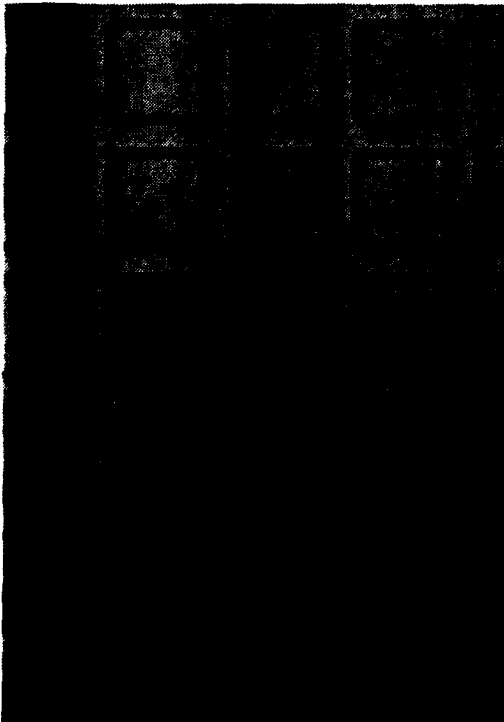
Micrographs of Etched HgCdTe Surface (200X) After Various Etch Times ($\text{H}_2\text{O}_2:\text{NH}_3$ 2:1, (a) 4 min, (b) 6 min, (c) 8 min, and (d) 10 min.



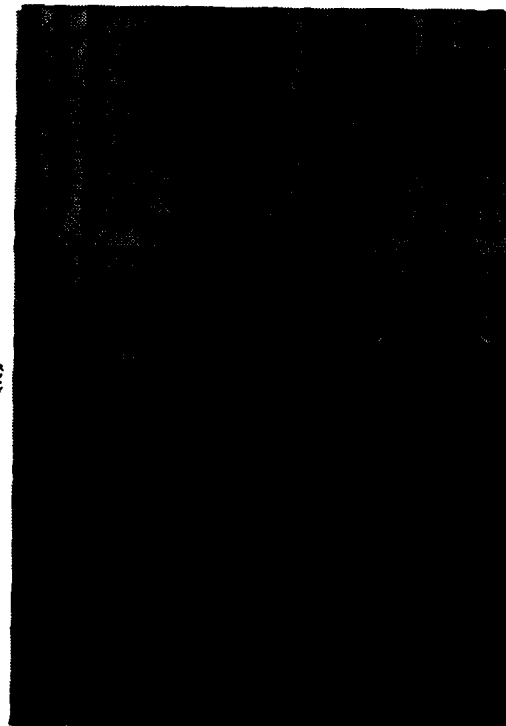
(a)



(b)

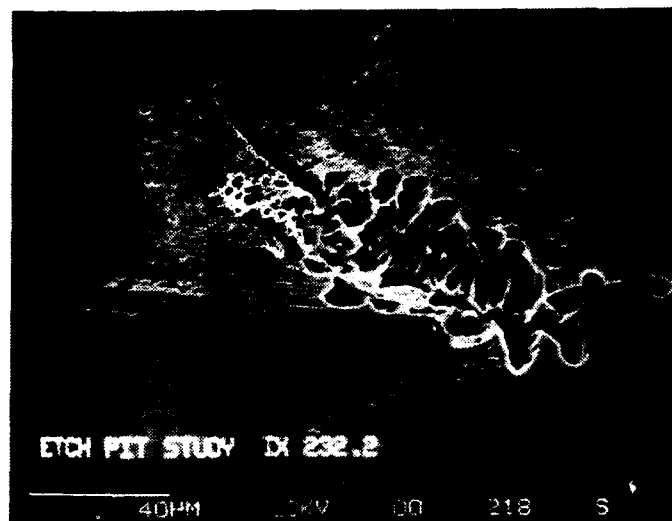


(c)



(d)

Higher Magnification Micrograph of Etched HgCdTe Surface (500X) After Various Etch Times
(a) 4 min, (b) 6 min, (c) 8 min, and (d) 10 min

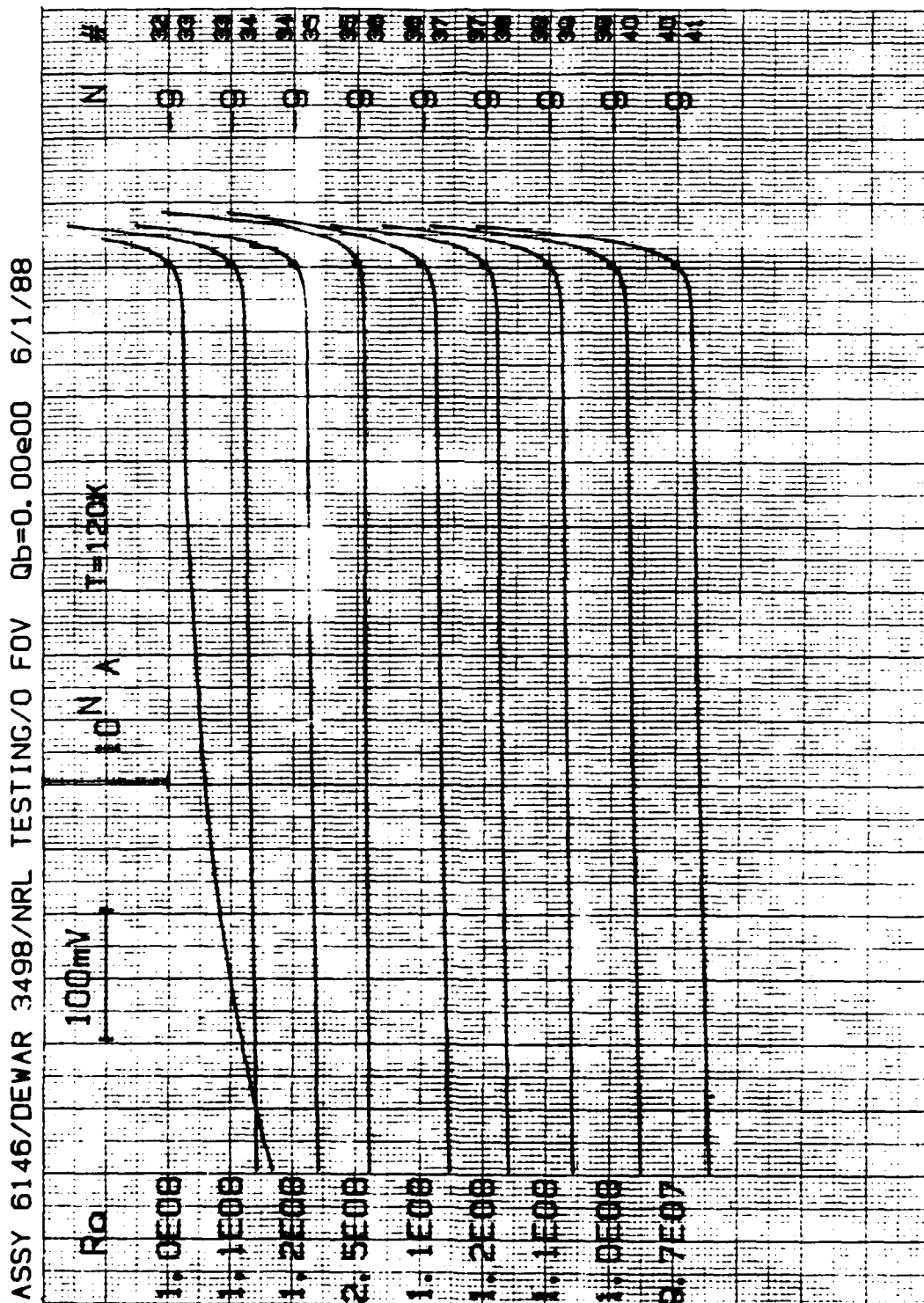


SEM Micrographs Showing Etch Pits on HgCdTe Surface After 10 Min Etch

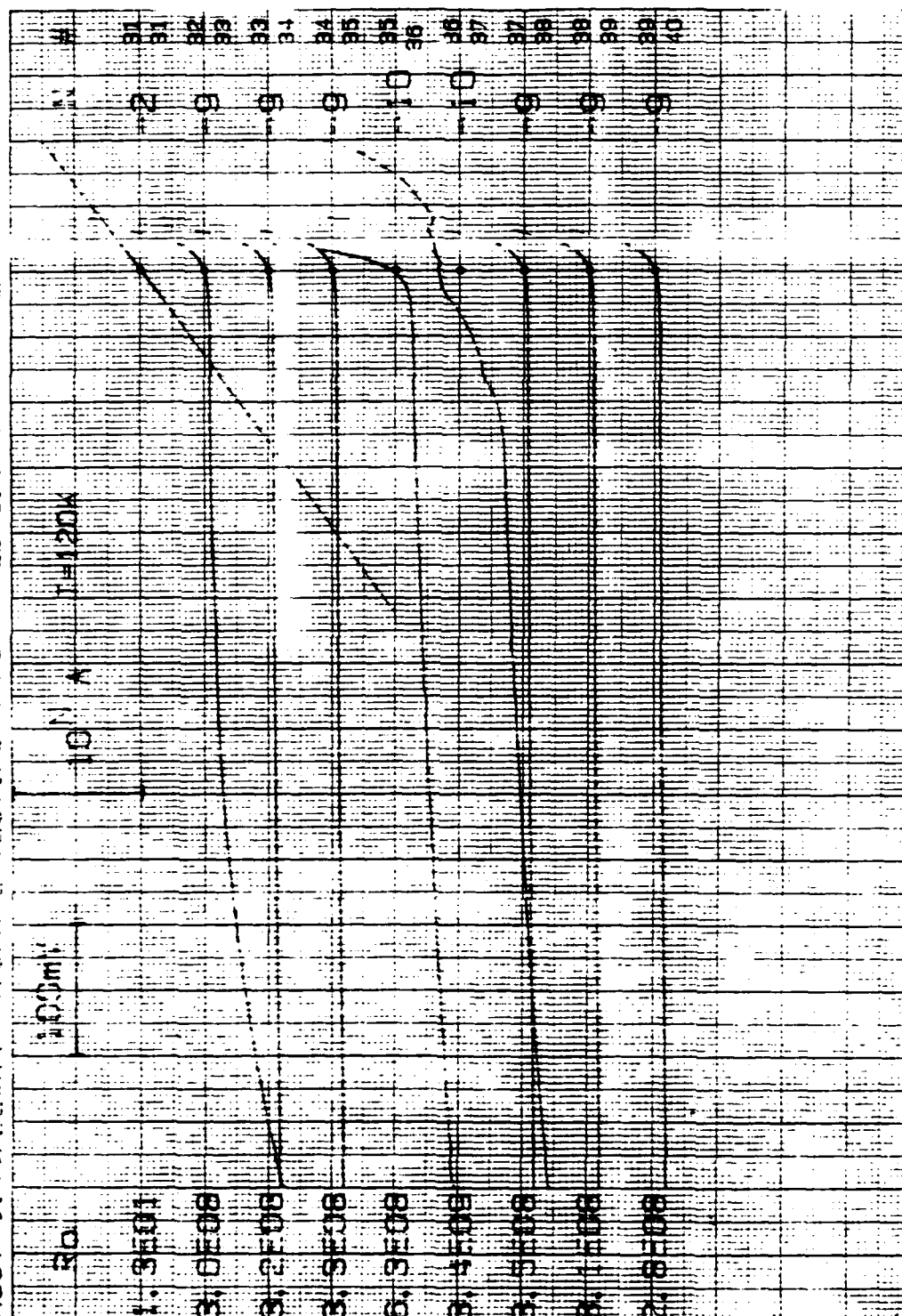
Appendix B

I-V CURVES AFTER 25 AND 200 THERMAL CYCLES

AFTER 25 THERMAL CYCLES



ASSY 6146, DEWAR 3498, PR. TESTING, 0.50% 0b=0.00e00 6'12'83



R₀A AND I-V SHAPE CHANGES FOR EACH DIODE

6537

Diode	1 t.c. R ₀ A	2 t.c. R ₀ A	3 t.c. R ₀ A	Change in I-V shape
9	1.2E9	3.1E9	9.1E7	
11	1.9E9	2.1E9	1.4E8	Yes
12*	1.8E9	3.7E9	2.5E9	
13*	1.6E9	3.3E9	2.4E9	
15*	1.4E9	3.2E9	2.2E9	
18	2.0E9	3.2E9	2.2E9	Yes
19	8.2E8	5.9E8	5.1E8	Yes
23	2.2E9	5.0E9	4.0E9	Yes
35	7.7E8	5.9E7	4.7E9	
46	4.9E9	5.2E11	6.8E9	Yes
51	4.7E8	1.1E9	1.7E8	Yes
55*	8.5E8	1.2E9	8.9E7	
61*	1.5E9	5.5E9	4.9E9	

* = control diodes

6131

Diode	1 t.c. R ₀ A	25 t.c. R ₀ A	Change in I-V shape
16	6.4E8	7.1E3	Yes
18	8.3E3	1.2E10	Yes
20	1.8E11	7.1E3	Yes
23	1.0E8	4.6E10	Yes
46	3.1E8	1.4E11	Yes

6508

Diode	1 t.c. R ₀ A	25 t.c. R ₀ A	Change in I-V shape
1	7.0E8	2.7E9	Yes
3	6.6E8	2.2E9	Yes
4	6.8E8	2.3E9	Yes
9	6.7E8	2.4E9	Yes
11	1.0E9	2.6E9	Yes
16	9.9E3	2.2E9	Yes
36	1.3E8	4.0E8	Yes
56	1.8E9	3.6E9	Yes
57	1.0E9	2.2E9	Yes

6146

Diode	1 t.c. R ₀ A	25 t.c. R ₀ A	200 t.c. R ₀ A	Change in I-V shape
1	1.8E8	1.2E8	3.2E10	Yes
3	1.8E8	1.1E8	4.4E10	Yes
5	1.8E8	1.1E8	8.6E10	Yes
9	7.0E10	6.4E10	2.8E10	Yes
17	1.6E8	8.7E7	2.3E8	Yes
18	1.6E10	8.6E7	2.0E8	Yes
37	2.1E8	1.1E8	3.4E9	Yes
57	1.4E8	9.6E7	2.9E10	Yes
64	1.2E8	1.6E11	3.6E10	Yes
65	1.8E8	9.3E7	4.6E10	Yes
68	2.0E8	1.1E8	8.6E10	Yes

6509

Diode	1 t.c. R ₀ A	25 t.c. R ₀ A	200 t.c. R ₀ A	Change in I-V shape
9		2.2E10	1.1E11	Yes
36	1.1E9	2.4E8	2.5E10	Yes
42	9.4E8	7.3E2	9.5E8	Yes
43	1.1E9	2.6E8	1.2E9	
48	1.0E9	2.3E8	9.3E8	
58	1.1E9	2.6E8	1.1E9	
64	1.4E9	6.6E10	9.7E10	Yes
65	1.4E9	2.2E10	8.5E10	Yes

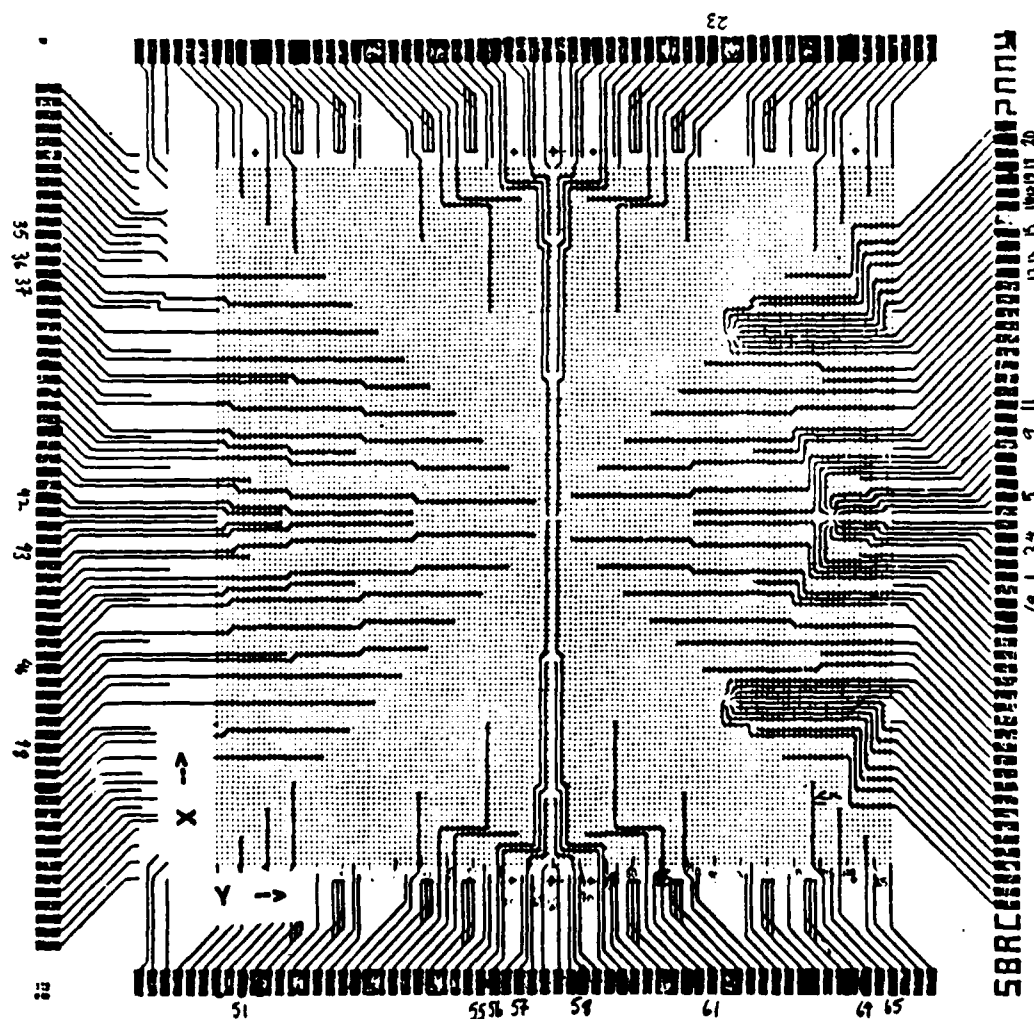
Appendix C

DIODE MAPPING LOCATIONS BY ASSEMBLY

Diodes which showed significant degradation with I-V testing:

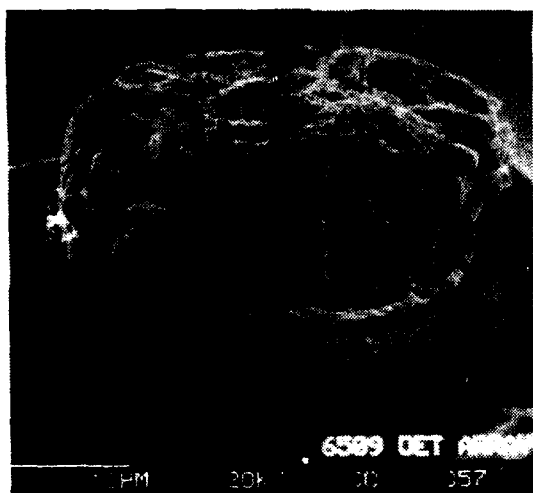
Assy 6537		Assy 6131		Assy 6508		Assy 6146		Assy 6509	
diode	grid	diode	grid	diode	grid	diode	grid	diode	grid
9	(71, 122)	16	(98, 99)	1	(63, 117)	1	(63, 117)	9	(71, 122)
11	(65, 91)	18	(99, 98)	3	(63, 118)	3	(63, 118)	36	(102, 1)
12*	(97, 97)	20	(98, 97)	4	(64, 118)	5	(65, 118)	42	(65, 13)
13*	(97, 98)	23	(102, 77)	9	(71, 122)	9	(71, 122)	43	(64, 38)
15*	(98, 98)	46	(46, 46)	11	(65, 91)	17	(99, 99)	48	(31, 31)
18	(99, 98)			16	(98, 99)	18	(99, 98)	58	(13, 65)
19	(99, 97)			36	(102, 1)	37	(98, 31)	64	(16, 113)
23	(102, 77)			56	(38, 64)	57	(13, 64)	65	(11, 118)
35	(108, 21)			57	(13, 64)	64	(16, 113)		
46	(46, 46)					65	(11, 118)		
51	(16, 16)					68	(63, 116)		
55*	(27, 76)								
61*	(27, 76)								

* = indicates control diodes on assembly 6537

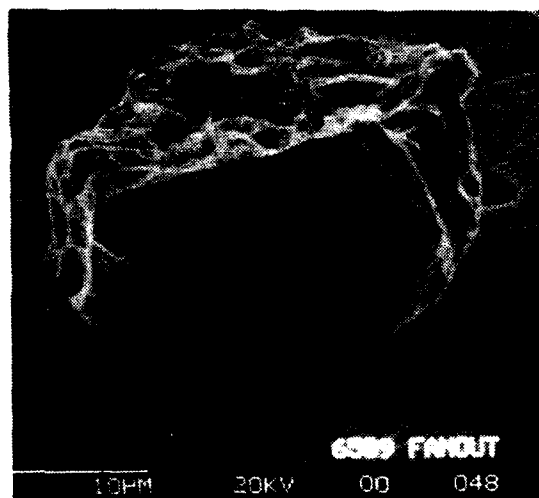


Appendix D

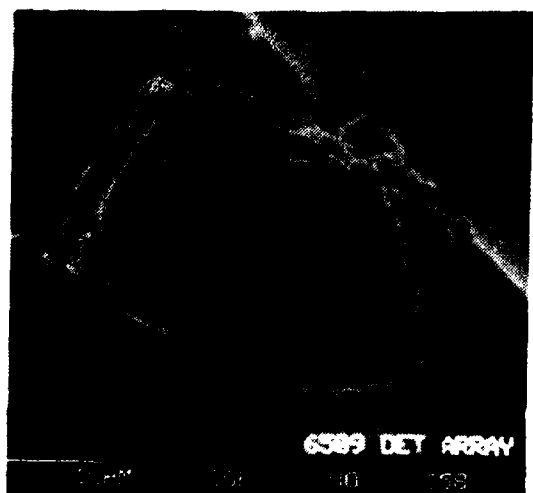
SEM MICROGRAPHS OF INDIVIDUAL DIODES TO FANOUTS



(a)



(b)



(c)

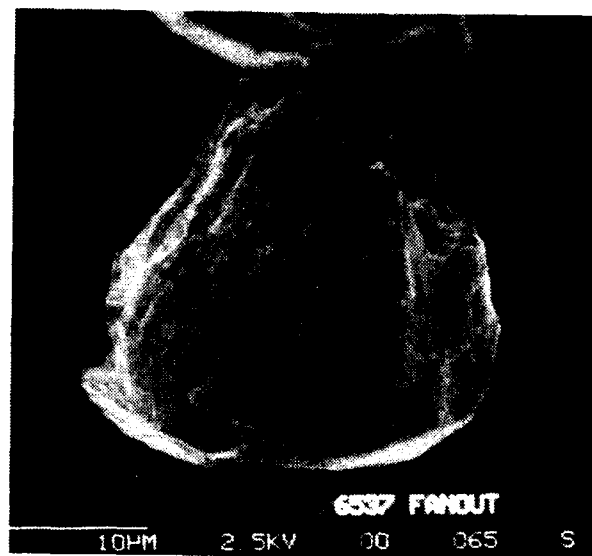


(d)

SEM Micrographs of Indium Bumps on Diodes and Fanout Metallization for (a) Diode 42 (b) Fanout for Diode 42, (c) Diode 43, and (d) Fanout for Diode 43



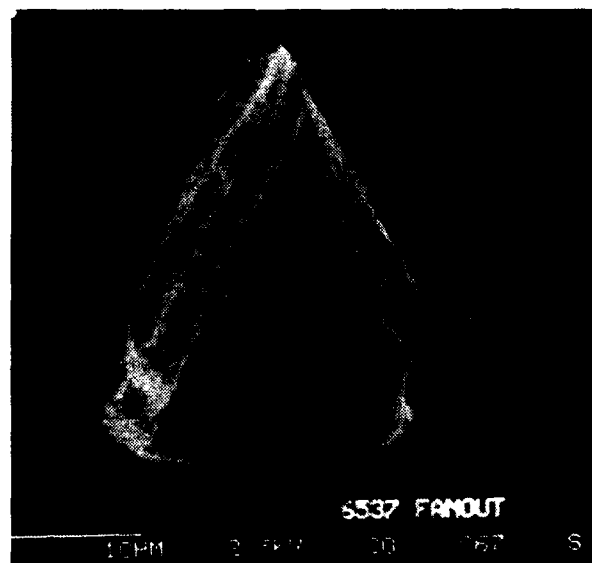
(a)



(b)



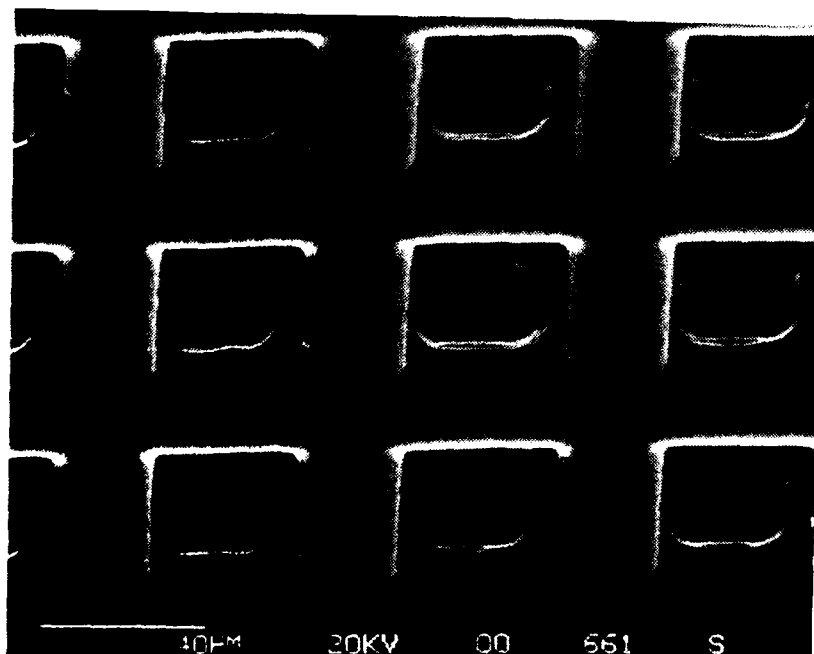
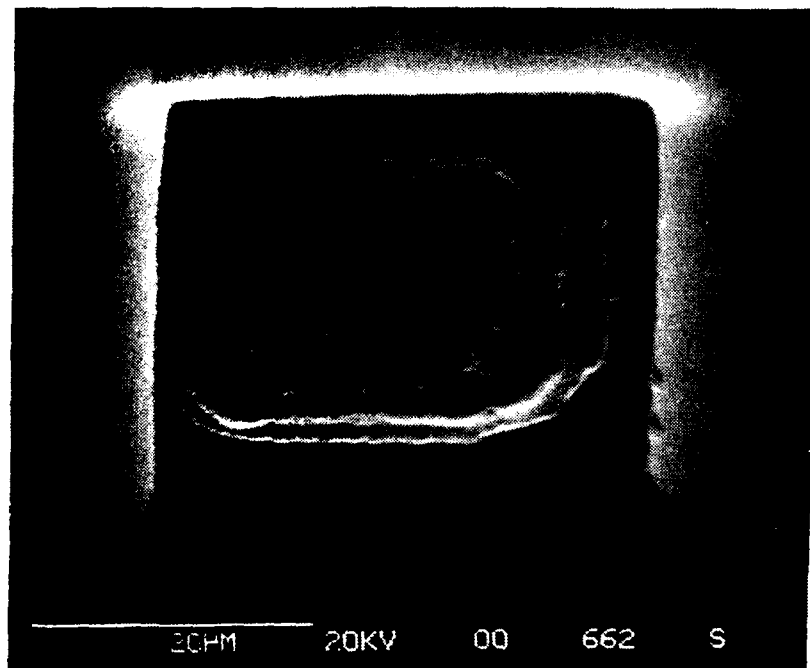
(c)



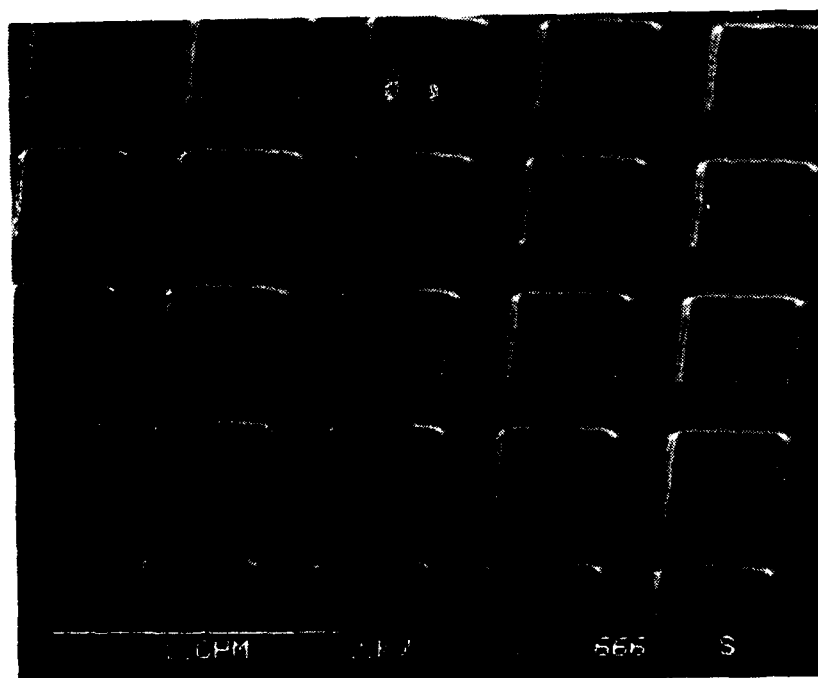
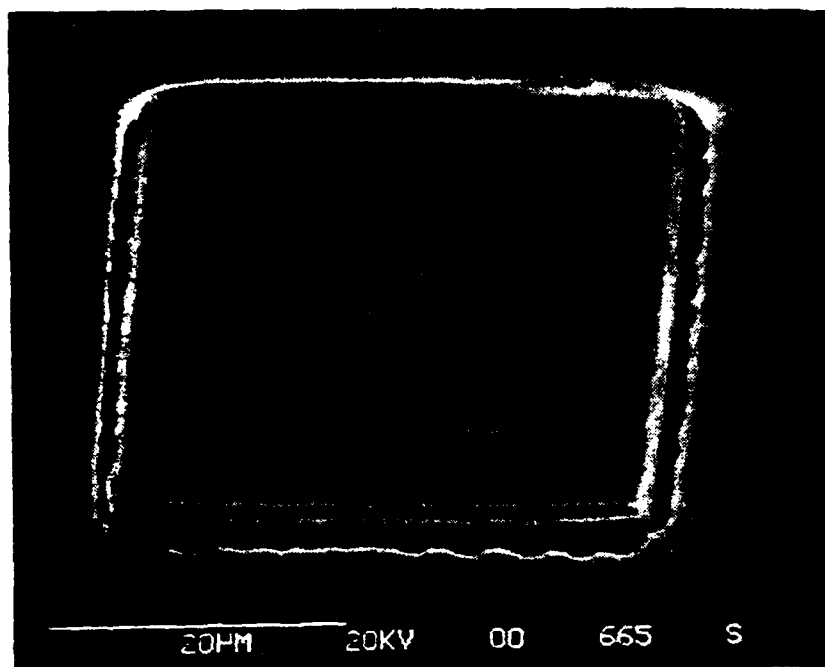
(d)

SEM Micrographs of Indium Bumps on Diodes and Fanout Metallization for (a) Diode 9 (b) Fanout for Diode 9, (c) Diode 11, and (d) Fanout for Diode 11

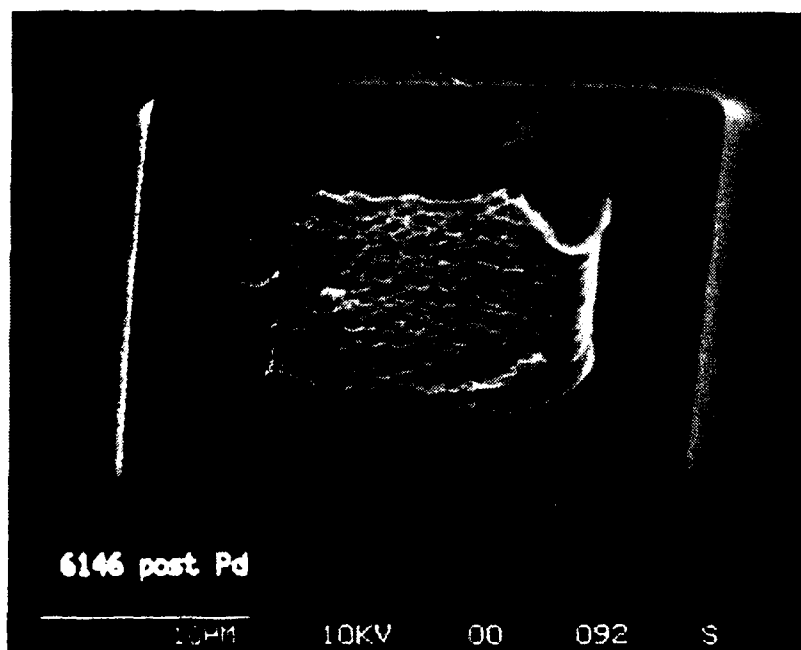
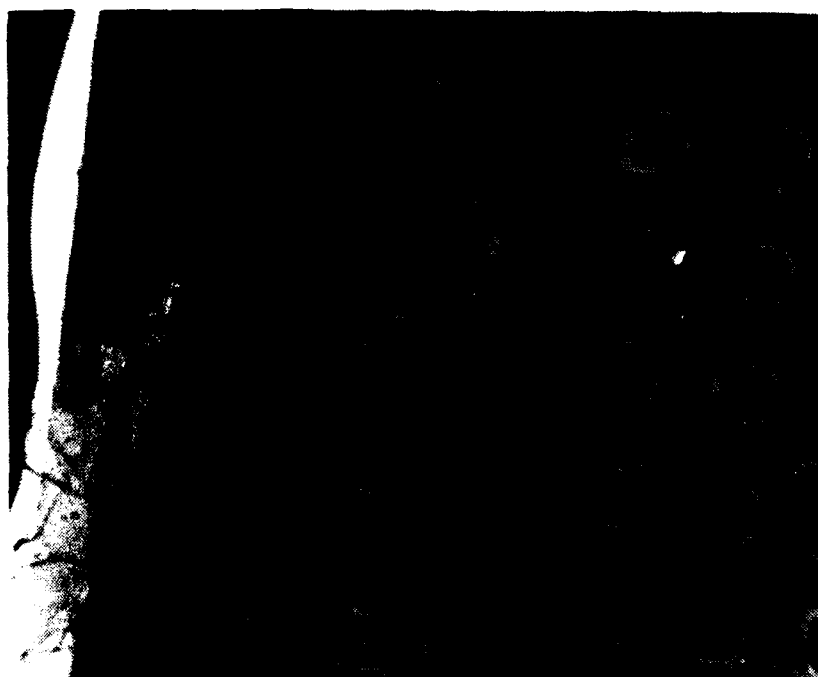
Appendix E
PALLADIUM ETCH RESULTS



SEM Micrographs of HgCdTe Mesa Diodes After Etching of Pd Metallization

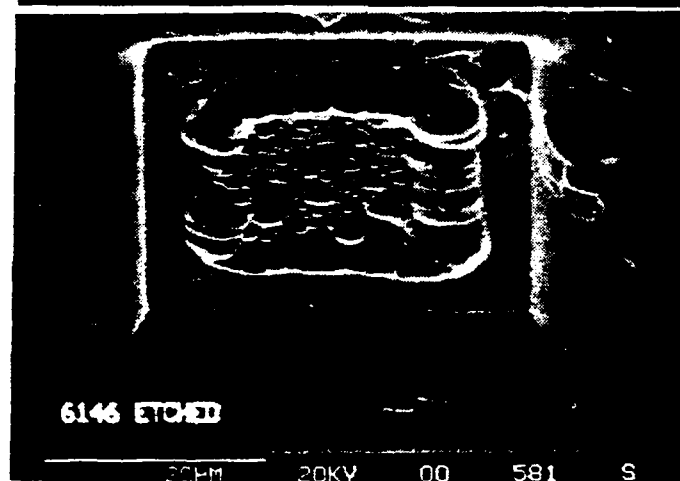
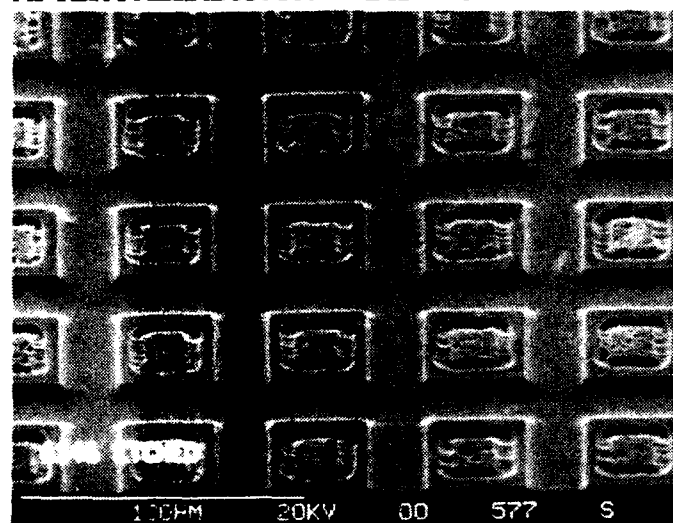


SEM Micrographs of HgCdTe Mesa Diodes After Etching of Pd Metallization



SEM Micrographs of HgCdTe Mesa Diodes After Etching of Pd Metallization

Appendix F
AFTER PALLADIUM AND DISLOCATION ETCHES



SEM Micrographs of HgCdTe Mesa Diodes After First Etching to Remove Pd and Then to Delineate Etch-Pits

Appendix G

X-RAY ANALYSIS DATA

An X-ray double-crystal rocking curve-analysis was performed on parts 6537 (control), 6131 (25 thermal cycles), and 6146, 6509 (200 thermal cycles). The "optimum" material would have a small full-width at half-maximum (FWHM). The results are shown below and summarized in Table G-1. It should be reiterated that the resolution of the x-ray analysis is limited, as it cannot evaluate individual diodes.

Table G-1. Peak Width for Each Assembly

Assembly	Thermal Cycles	FWHM (arc-sec)
6537	3	96
6131	25	56
6146	200	99
6509	200	37

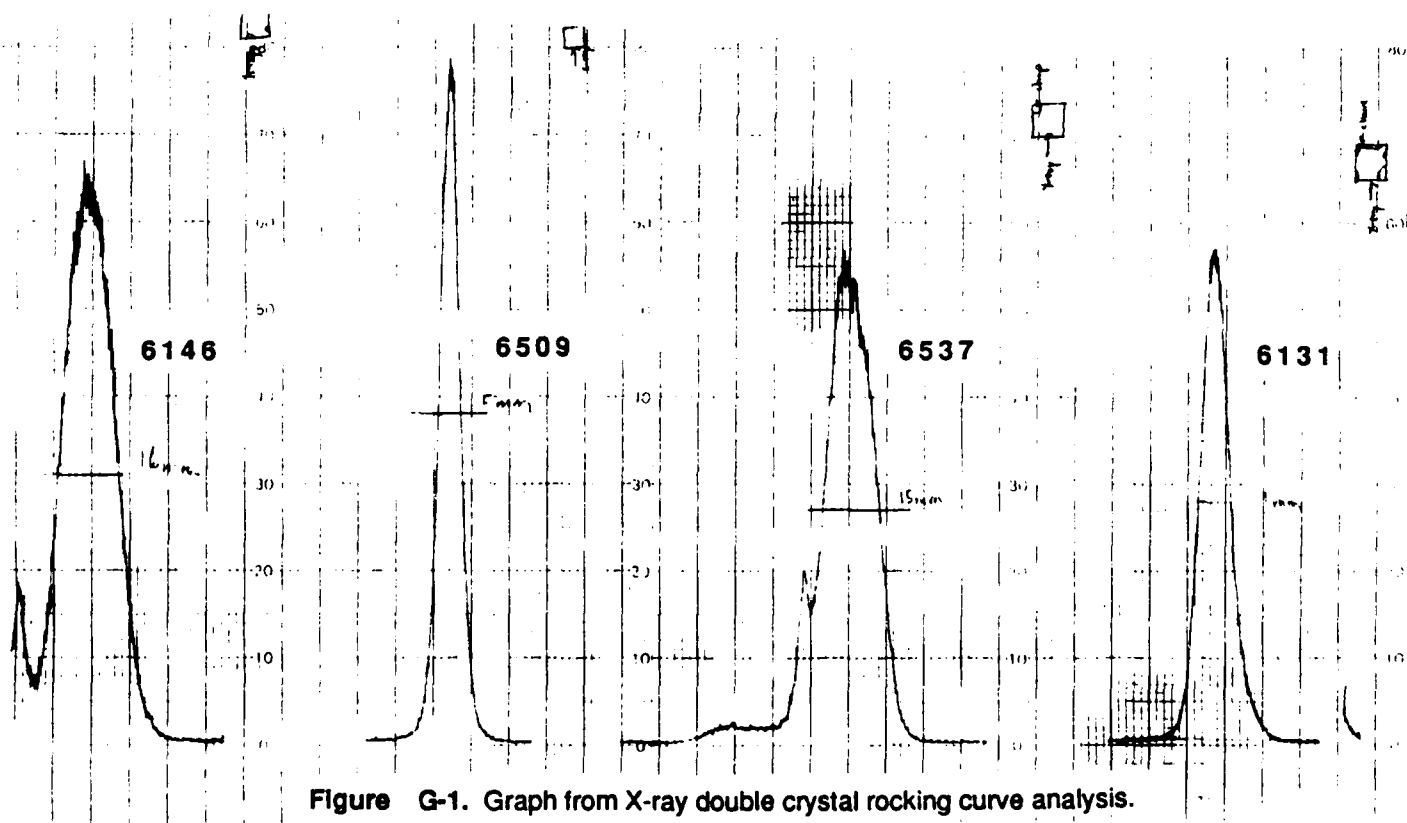


Figure G-1. Graph from X-ray double crystal rocking curve analysis.